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JUNE 3, 1985
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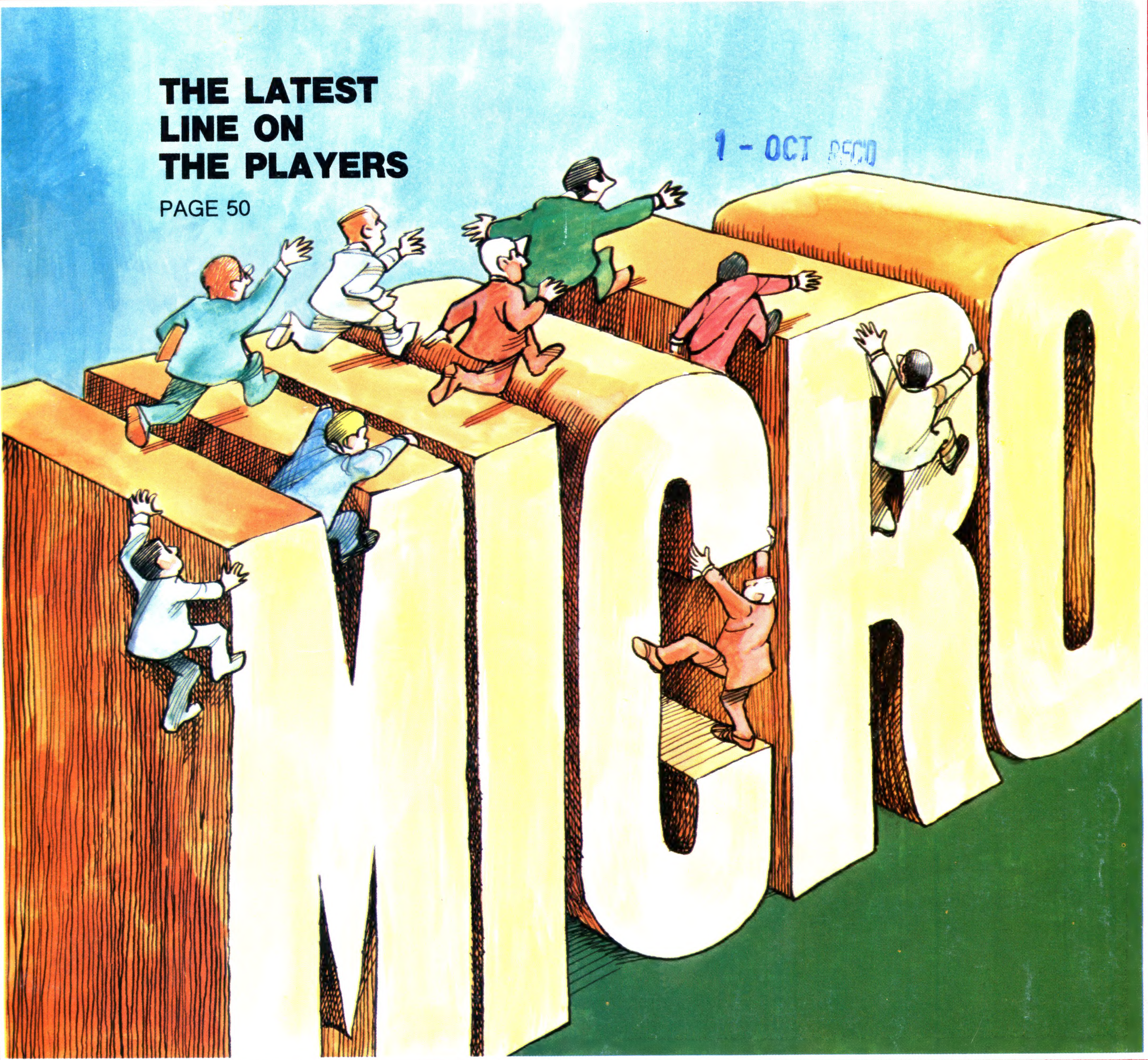
ElectronicsWeek

THE MAGAZINE OF THE WORLDWIDE ELECTRONICS INDUSTRY

THE 32-BIT RACE GETS CROWDED



THE LATEST LINE ON THE PLAYERS
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Fuzzy logic gets a strong push from AI-system designers/40

Electrically erasable logic slashes programming time/56

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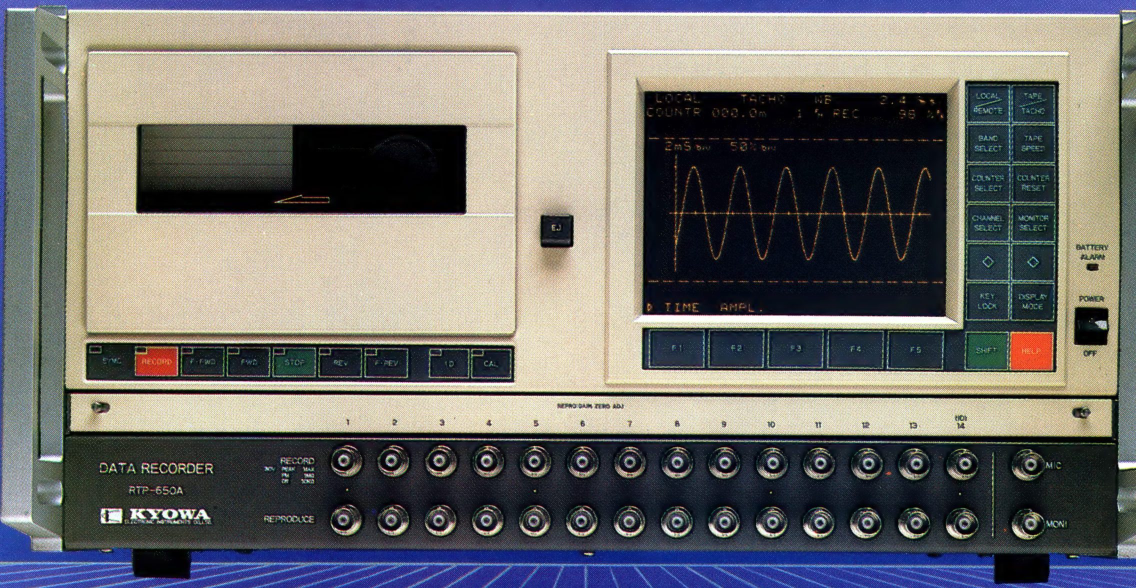

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International edition

PREVIEWS

Next ElectronicsWeek

The last word on voice-synthesis systems

Uses for voice output such as time and weather information by telephone are not new. Until recently, however, these services have mostly been recorded on tape. But now synthesized speech is inching to center stage. It can be heard in elevators, trains, and cars, providing warnings and messages formerly announced by humans or provided on displays. For the latest in speech-development systems—this one for use with a personal computer—see the next issue of *ElectronicsWeek.*

Busy days lie ahead for the relay industry

There is action aplenty in the electromechanical relay business these days. Thanks to new materials, innovative packaging, and more automated manufacturing, today's relay has been substantially decreased in both size and cost. Further spurred by increased Japanese investments and innovation, progress in the relay industry is marked by the ability to cultivate new applications and to develop a new generation of relays based on photovoltaics, integrated-circuit technology, and hybridization. For a rundown of the latest developments and what they mean, see the next issue of *ElectronicsWeek.*

Looking ahead in ElectronicsWeek

Dream versus reality in automotive electronics

Has the electronic revolution under the hood and in the passenger compartment of the automobile that has been so optimistically forecast for the past decade actually come to pass? The talk about the new market for electronics ranges from sensors planted inside the engine to space-age displays replacing the dials and gauges of the conventional dashboard; a June 17 special report will examine the dream and its fulfillment.

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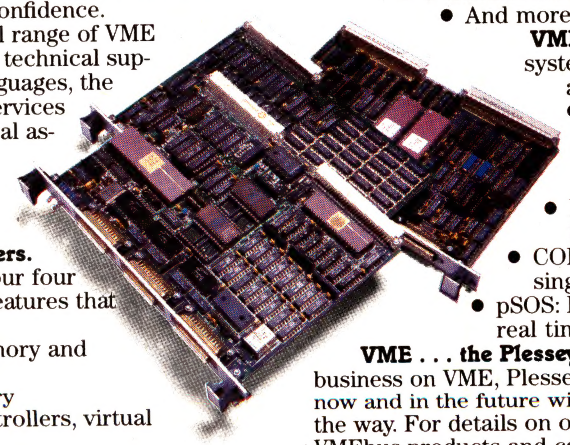

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PROGRAMMABLE LOGIC PARTS

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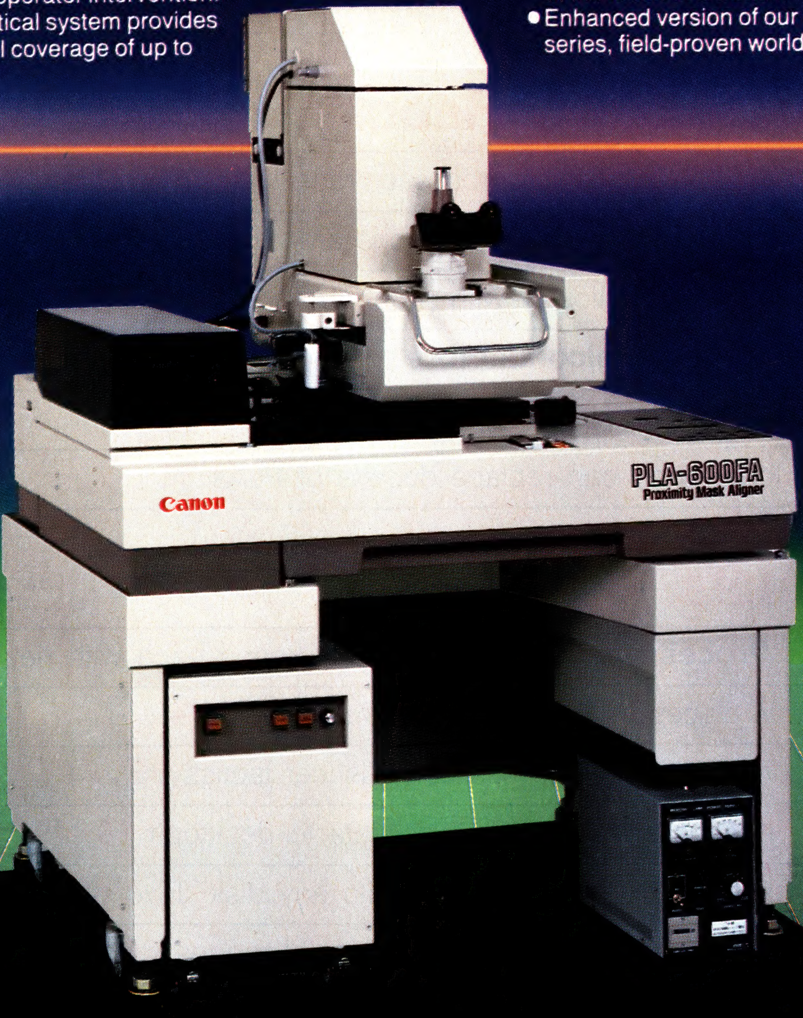

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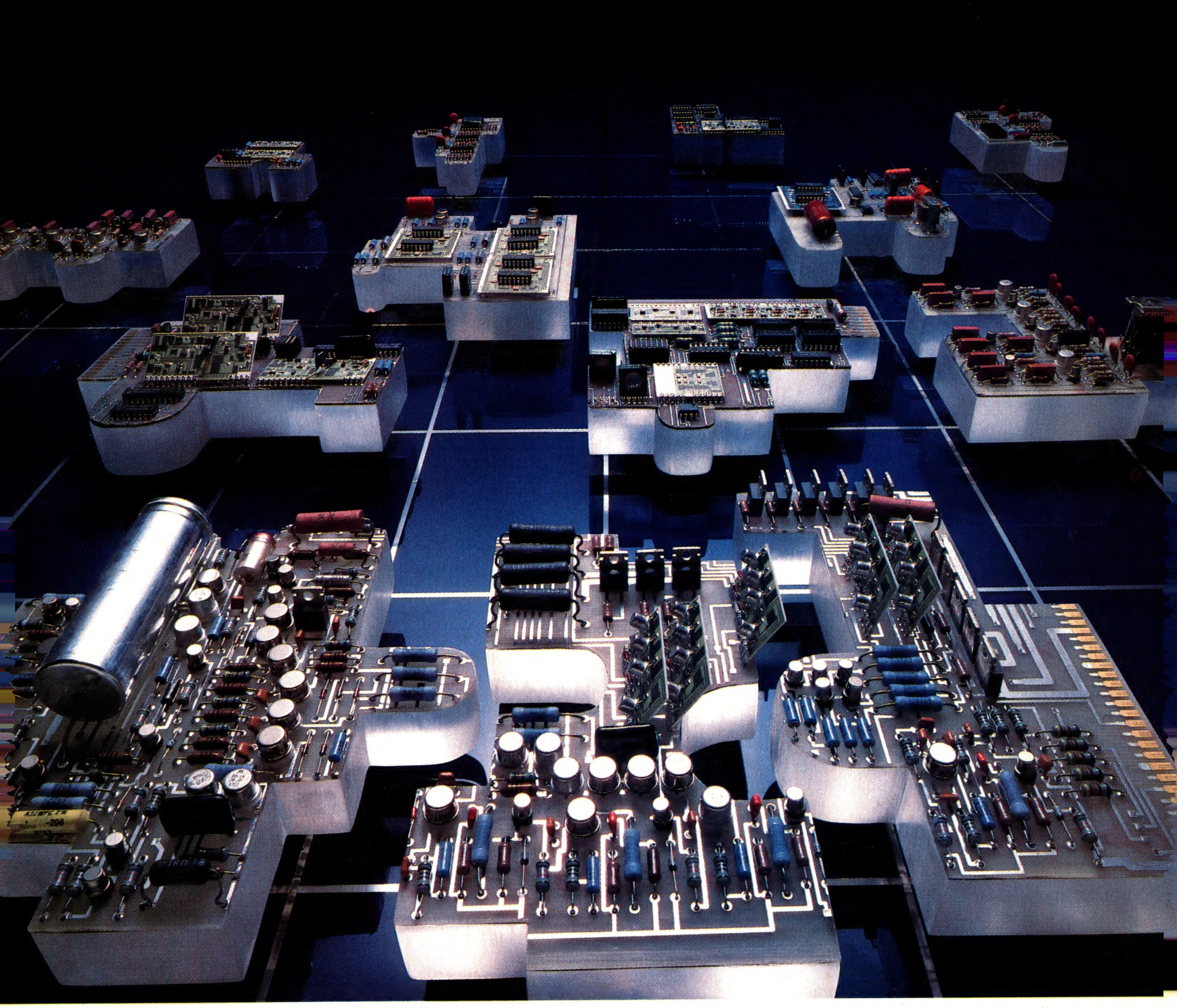

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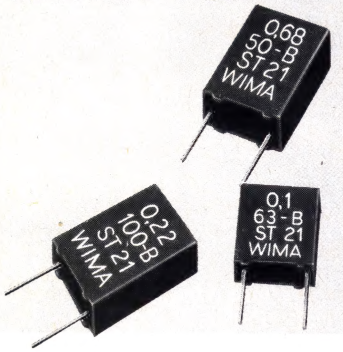

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MEETINGS

International Conference: Post Failure Analysis of Fiber Reinforced Composites, Air Force Wright Aeronautical Laboratories (Faye Geidner, Conference Coordinator, 1616 Mardon Dr., Dayton, Ohio 45432), Stouffers Hotel, Dayton, Ohio, July 1-3.

Laser '85—Opto-Electronic International Congress, Munich Trade Fair Corp. (Postfach 12 10 09, D-8000, Munich 12, West Germany), Munich Trade Fair Central, Munich, July 1-5.

World Computer Graphics '85 Exposition and Conference, World Computer Graphics Association and the National Computer Graphics Association (American Communications Group, 8300 Greensboro Dr., Suite 690, McLean, Va. 22102), New York Coliseum, July 10-12.

Computex Taipei '85, China External Trade Development Council (Taipei Sungshan Airport, Taiwan, Republic of China), CETDC Exhibition Complex, Taiwan, R.O.C., July 12-18.

Annual Powder Metallurgy Conference & Exhibition, Metal Powder Industries Federation and the American Powder Metallurgy Institute (MPIF, Princeton Forrestal Center, 105 College Rd. E., Princeton, N.J. 08540), Fairmont Hotel, San Francisco, July 14-17.

Micro Security '85, Computer Security Institute (Russell Kay, CSI, 43 Boston Post Rd., Northborough, Mass. 01532), Marriott Crystal Gateway, Arlington, Va., July 15-16.

National Computer Conference, American Federation of Information Processing Societies (1899 Preston White Dr., Reston, Va. 22091), McCormick Place, Chicago, July 15-18.

Drives/Motors/Control Show, Incremotion Associates Inc. (550 Saint Charles Dr., Suite 107, Thousand Oaks, Calif. 91360), Olympia 2 Convention Center, London, July 16-18.

AT&T & IBM: New Directions in Technology, Eastern Management Group (Four Century Dr., Parsippany, N.J. 07054), Plaza Hotel, New York, July 17-18.

SCSC '85—1985 Summer Computer Simulation Conference, Society for Computer Simulation (P.O. Box 17900, San Diego, Calif. 92117), Westin Hotel, Chicago, July 22-24.

International Symposium on Microwave Technology in Industrial Development, Brazilian Microwave Society (Jose Giarola, Telebrás Research and Development Center, 13100 Campinas, São Paulo, Brazil), Telebrás Research & Development Center, São Paulo, Brazil, July 22-25.

Siggraph '85—The Twelfth Conference on Computer Graphics and Interactive Techniques, Association for Computing Machinery and IEEE (Siggraph '85 Conference, Services Office, 111 E. Wacker Dr., Chicago, Ill. 60601), San Francisco, July 22-26.

Seminars

Applying Advanced Digital Communications, Technical Marketing Society of America (Technology Training Corp., P.O. Box 3608, Torrance, Calif. 90510-3608), Bethesda Marriott Hotel, Washington, July 1-2.

Advanced Technologies & Marketing Strategies for Local-Area Networks, Technical Marketing Society of America (Technology Training Corp., P.O. Box 3608, Torrance, Calif. 90510), Wyndham Hotel, Orlando, Fla., July 1-2.

Digital PBXs, Systems Technology Forum (9000 Fern Park Dr., Burke, Va. 22015), Barbizon Plaza Hotel, New York, July 8.

Flow Visualization Techniques: Principles and Applications, University of Michigan (200 Chrysler Center, North Campus, Ann Arbor, Mich. 48109), University of Michigan, Ann Arbor, Mich., July 8-10.

Local-Area Network Markets, Information Gatekeepers Inc. (214 Harvard Ave., Boston, Mass. 02134), Hyatt Regency, Crystal City, Va., July 9.

Applied Digital Signal Processing, Union College (Graduate and Continuing Studies, Wells House, 1 Union Ave., Schenectady, N.Y. 12308-2363), Union College, Schenectady, N.Y., July 9-11.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Micro Systems Institute (Garnett, Kan. 66032), Ramada Inn at San Francisco International Airport, Burlingame, Calif., July 9-12.

Workshop on Wafer-Scale Integration, University of Southampton (WSI Workshop Secretary, Department of Electronics and Information Engineering, University of Southampton, Southampton, SO9 5NH, England), University of Southampton, July 10-12.

THIS ElectronicsWeek

THURSDAY *May 23*

Allen-Bradley Co. unveiled a **computer-integrated manufacturing facility it says can produce 600 motor starters per hour.** The 45,000-ft^2 "factory in a factory," built for $15 million, showcases the firm's manufacturing automation equipment on one floor of Allen-Bradley's nine-story Milwaukee factory. The facility requires no direct labor, only a crew of three or four to monitor its control room. Allen-Bradley said the system will permit inventories to be kept at a minimum because production lead time is only one day.

FRIDAY *May 24*

Making yet another aggressive sales move in the personal computer market, **IBM Corp. slashed prices on two slow-moving models:** the Portable Personal Computer and the PCjr, which was recently pulled out of production. The orphaned 128-K-byte PCjr with one floppy-disk drive now lists for $725, 27.4% below its previous list price. Big Blue cut prices 24.8% for its standard 256-K-byte Portable PC with a single floppy-disk drive, to $1,950; its model with dual floppy-disk drives now lists for $2,250, 22.2% below previous levels. According to IBM, it is premature to speculate that the price cuts indicate plans to cancel the Portable PC. "Sales have slackened, but it's still a fully supported member of our PC family," said a company representative.

MONDAY *May 27*

As most of the nation flocked to beaches and parks for Memorial Day, **Lotus Development Corp. quietly began shipments of its long-awaited Jazz software package.** Jazz, an integrated business program considered by many to be vital to the success of Apple Computer Inc.'s Macintosh 512-K personal computer, will retail for $595. Introduced in November for March release, development problems delayed delivery by two months.

TUESDAY *May 28*

Uniform Software Systems Inc. said it developed **an add-on program for Lotus 1-2-3 that nearly doubles the usable spreadsheet memory** by allowing it to run in protected-virtual-address mode on IBM Corp.'s Personal Computer AT. Called The Extender, the program increases the maximum usable memory from about 500-K bytes to 920-K bytes. It will be available in July for $99. Lotus Development Corp., which wrote the 1-2-3 program, and Intel Corp. announced in April that they were jointly developing a similar product for delivery in the fall. . . . **General Electric Co. cut required lead time for power MOS FETs by more than half,** to a maximum of 12 weeks. GE said the improved turnaround was a result of improved efficiency at its wafer-manufacturing plant in Syracuse, N.Y.

WEDNESDAY *May 29*

Leaping head-first into the office-automation market, **Eastman Kodak Co. unveiled an electronic-publishing and an image-management system.** The image-management system permits office personnel to retrieve documents on microfilm almost instantly from a computer work station, utilizing a complex local-area network, robotics, and charged-coupled-device scanners, to retrieve and digitize the stored image. The system is designed to accommodate optical-disk recorder/players in the future for high-density image storage and retrieval. The Ektaprint electronic publishing system, Kodak's first thrust into electronic publishing, can merge text and graphics to produce documents of near-typeset quality. □

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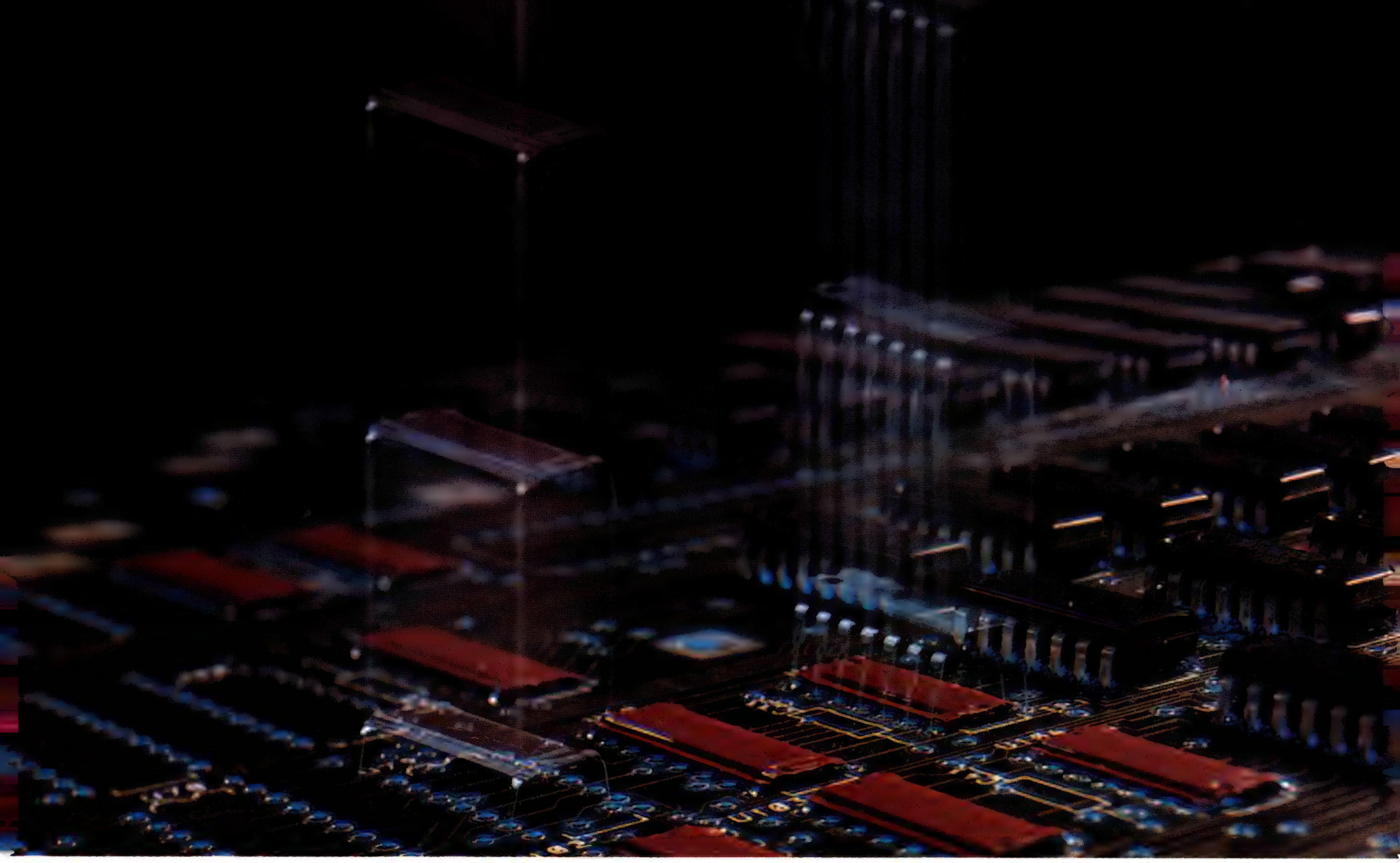

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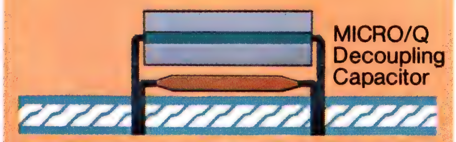

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UP FRONT

Electronics industry is favorable toward Reagan tax plan

Electronics and computer companies, along with other high-technology outfits, should turn out to be winners under President Reagan's proposed tax reform. Industry and government officials surveyed last week agreed that the plan favorably addresses issues important to the electronics industry. These include reduction of the top capital gains rate from 20% to 17.5% and a three-year extension of the research and development tax credit. "We expect to work aggressively for the bulk of the package," says Ralph Thomson, senior vice president of public affairs for the American Electronics Association in Palo Alto. Silicon Valley's man on the Hill, Rep. Ed Zschau, R-Calif., agrees "that the major hopes of the industry were met. The major improvement of Treasury II over Treasury I is a much greater emphasis on capital formation." Despite the proposed extension of the R&D tax credit that is set to expire this year, Thomas B. Patton, executive director of legislative affairs for the Electronic Industries Association, says, "We'd like very much for the tax credit to be permament." Other segments of the proposal drawing industry praise are the restoration of tax-free employer-provided education benefits and tax-deferred incentive stock options. The remaining question is whether the tax proposal, in its present form, will fly at all this year. ☐

Sony adds pcm sound to video cassette recorders

Sony Corp. has taken a quantum leap forward with a home video cassette recorder, the EV-S700, that incorporates stereo pulse-code modulation capability for the sound accompanying the video it is recording. It also features multiple facilities to record six separate pcm audio tracks. Frequency range is flat to 15 kHz and automatic noise reduction gives a dynamic range of 88 dB. In addition to hi-fi sound, the VCR provides the largest choice of display options among Sony's 8-mm VCRs, including frame-by-frame display, slow motion, and double speed—all for $993 (see related story, p. 27). ☐

FCC to reexamine code and protocol conversion in Computer Inquiry III

Watch this month for the Federal Communications Commission to begin rewriting the definitions of basic and enhanced services defined by Computer Inquiry II, the landmark investigation that led to the breakup of the Bell System's telephone monopoly. As telephony during the 1970s began to assume many of the aspects of digital data processing, the FCC came up with a set of regulations—still in force—to keep the monopoly from competing with value-added networks and data-processing outfits. Yet some code and protocol conversion is deemed essential to packet transmission, which one FCC aide called "the wave of the future" for data and voice transmissions. So a reexamination by the Common Carrier Bureau is in the offing, and may signal the start of yet another investigation. ☐

French and Japanese battle over smart-card standards

A battle between French and Japanese manufacturers of smart cards—credit-type cards containing one-chip microcomputers—has broken out over where to physically implant the chip. According to the Groupement Carte à Mémoire (GCM), a group based in Paris that was established by French banks to promote the cards, Japanese manufacturers are asking the International Organization for Standardization to standardize implantation somewhere near the middle of the card instead of at the upper right-hand corner, as favored by the French. GCM claims the Japanese manufacturers are trying to avoid being forced to move three magnetic stripes, currently deposited where the French circuit resides (see related story, p. 44). ☐

UP FRONT

Star Technologies to market superprocessor for high-performance CAE

Convinced that current computer-aided-engineering systems are computer-bound and take care of only the human interface to systems design, Star Technologies Inc. will up the ante on work stations by developing a super-powered CAE design system. Star, an array-processor manufacturer based in Portland, Ore., will deliver papers at the late-June Design Automation Conference in Las Vegas describing its internal CAE experience and its plans to enter the CAE market with a product intended to achieve accurate design of complete systems on the first pass. Star designed its emitter-coupled-logic-based ST-100, which handles 100 million floating-point operations/s, by first simulating the entire system on a Cyber 176 supercomputer. It took 700 hours of central-processing-unit time but resulted in the design of 18-gate arrays on three boards without a single error, says Bob Hausman, vice president of advanced development. Systems will be available in late 1986. ☐

Alpha Industries earns reinstatement with Pentagon

Alpha Industries of Woburn, Mass., suspended by the Pentagon earlier this year after a kickback indictment last fall involving alleged payments for a Raytheon Co. subcontract, has reached a settlement that will allow it to resume business with the military. Under terms of the agreement, Alpha will plead guilty to one count of violating anti-kickback laws and pay fines totaling $97,000. In addition, Anthony J. DeCarolis, a vice president named in the indictment has been fired, and Alpha's chief executive officer and president, Andrew Kariotis, will be removed from office for a year. His brother, George, will take over as CEO. Alpha specializes in microwave and millimeter-wave components and has in the past done 70% of its business with the military. ☐

Home computer crisis catches up with Sinclair

Sir Clive Sinclair has bowed to the inevitable and decided to step down as CEO of Sinclair Research Ltd., the UK's leading computer maker. Thus, the troubled British personal computer market claimed another casualty; earlier this year, Ing. C. Olivetti & C. SpA took a half share in Acorn Computers Ltd. for a mere $12.8 million. Neighboring Sinclair has been suffering similar cash-flow problems and asked suppliers for extended credit. Sinclair has suffered from poor sales of its mainstay Spectrum computer and the more expensive $500 QL computer. And although his C5 electric tricycle is a separate venture, its flop has damaged Sinclair's credibility among investors, hardly offset by promising production of the company's $125 black and white pocket TV. Sinclair says it will seek outside financing, which will force Sir Clive to sell off a large part of his 85% share in his namesake company. ☐

New player joins X-ray lithography crew

X-ray lithography markets could boom as much as fiftyfold over the next four years, and a new player—Hampshire Instruments, of Rochester, N.Y.—has entered the game, filling a slot vacated in April by Varian Associates. Other firms in the field include Micronix Corp., Perkin-Elmer, and the Japanese companies Nikon and Canon. Normally secretive, Micronix revealed at the late-May Semicon West meeting that it had experimented successfully with additive masks (subtractive masks are the norm) that make possible 0.5-μm features having vertical wall profiles. For its part, Hampshire has revealed that its X-ray source will be a laser plasma generator using focused laser radiation. This results in a source with extremely bright and intense X-radiation. This in turn makes possible extremely short exposure times, a factor needed for high throughput. ☐

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SILICON FOUNDRIES WARM UP TO WORK-STATION ROUTING

New design-automation software reduces concern about chip designers' physical layouts

Austin, Texas

In the fabrication of semicustom chips, much grief can come if the physical layout of interconnections isn't right on the button. As a result, foundries traditionally have preferred to work up the routings themselves from the chip designers' network lists.

But now, vendors of design-automation software are striking up much closer relationships with major silicon merchants. Developments in layout-auditing software, rule-based expert-system techniques, and the proliferation of standalone work stations are finally nudging the industry into wider use of automatic-placement and -routing programs.

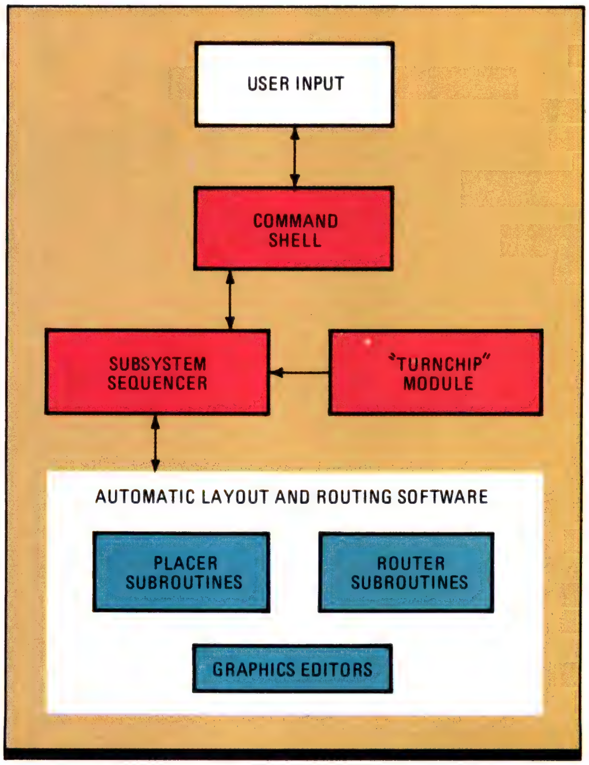
Using an expert system to fine-tune algorithms for automatic routing, VR Information Systems Inc. of Austin is now employing new rule-based software modules to quickly tailor the layout subroutines of its Merlyn-G layout package for specific silicon foundries and gate-array products. A key addition to the Merlyn-G layout package is a subsystem-sequencer program that launches in correct order subroutines for device placement, interconnection routing, and physical design checking.

Command shell. The manner in which the arsenal of subroutines is launched is based on rules in a software module called Turnchip (see drawing). The work station operator interfaces to the automatic-layout package through a menu-driven command shell.

Layout strategies and process design rules for specific gate-array products are loaded by VR Information Systems into the Turnchip modules, which represent the combined knowledge of the company's Merlyn programmers and the chip-layout experts at the integrated-circuit firm. As a result, VR Information Systems will be promoting the new chip-layout packages as "foundry-endorsed" computer-aided-design software, states W. Kelly Rupp, product marketing manager at the Tektronix Inc. subsidiary.

Slated for public debut later this month at the Design Automation Conference in Las Vegas, the first Turnchip module has been created for RCA Corp.'s PA50000 series of CMOS gate arrays. Turnchip is available on work stations from Apollo Computer Inc. and Valid Logic Systems Inc. as well as minicomputers and mainframes from Digital Equipment Corp. and IBM Corp. The cost of packages will range from $800 for small-gate-count arrays to $7,700 for larger designs.

Replacing experts. Other semicustom-chip vendors are also working with VR Information Systems to create Turnchip packages for their product lines and processing technologies, says Rupp.



The route stuff. VR Information Systems software—the command shell, the subsytem sequencer, and the Turnchip module—automates physical layout of semicustom chips.

"Until this, it generally took an expert to run Merlyn-G, and this replaces the need for an expert," he adds, referring to the vast number of options and layout strategies contained in the raw form of the automatic-layout package.

To RCA, the Turnchip module is just one of several closer working relationships between the firm and CAD software vendors. "If there is a trend, it is work stations moving toward more physical layouts, in both gate arrays and standard cells," notes Henry F. Miiller, manager of RCA's Semicustom Design Centers.

Automatic-layout packages generally have been tailored for each master logic array and the associated processing technology. Often, chip suppliers set tuning switches to optimize routing strategies and algorithms for geometries of the semicustom products.

"Various chip makers have supported and warmly embraced physical routing software, and others have stood back from that movement. We feel we are in harmony with the growing trend," states Miiller.

"But you have to be selective about whom you embrace because the chip maker, the customer, and work-station firm can get black eyes if the software does not route chips as promised," he points out. RCA has developed a sophisticated backend-checking system that audits physical designs executed by automatic-layout packages.

Also working closely with RCA has been Daisy Systems Corp. of Sunnyvale, Calif., which approaches automatic-layout software as a joint venture with silicon houses. "We have developed a generic technology for placement and routing aimed at various technologies, such as CMOS and bipolar approaches," says Tony Zingale, marketing manager for semicustom products. Parameters for specific products are set before delivery of software to gate-array customers.

Daisy's Gatemaster layout software has been on the market for two years, and this year the firm is starting to see a shift in general support for automatic-routing packages from major IC companies, according to Zingale. Motorola Inc.'s bipolar gate-array operation in Phoenix, Ariz., for example, has begun working with Daisy on tuned Gatemaster software for its products. Emerging interface standards such as the Electronic Design Interchange Format (EDIF) and wider use of work stations by both designers and chip makers are all helping to encourage greater use of computer-generated physical routing programs, Zingale believes.

Still, as much as 98% of today's gate-array designs are actually routed by semiconductor engineers at the silicon foundry, counters Michael Turner, vice president of Metheus CV Inc. of Hillsboro, Ore. "For most customers, it is still a matter of not having money for software. And the silicon foundry wants the security of doing the physical design from netlists from the customer's front-end work, such as schematic capture."

The Turnchip module and subsystem sequencer operate together much like a microcode-based state machine, automatically working their way through a number of Merlyn-G subroutines, explains Kevin Morris, a member of the technical staff involved in its development. The system will typically start off with a placer that checks the location of devices. Following this step, a global router will usually allocate routing resources. If congestion is detected, the placer routine can be called in to reposition a device.

The subsystem sequencer, written in Fortran 77, runs the design through the iterative layout, route, rip-up, and reroute subroutines until the gate-array design meets the specifications of chip customer and producer. The process runs automatically: all the work-station user has to do is push a button to start it running. *–J. Robert Lineback*

SOFTWARE

NEW SOFTWARE MEDIUM LOOKS LIKE CREDIT CARD

Tokyo

Although it looks like a fat credit card, it isn't used at a store, but rather as a store.

The card is a new way to distribute game and program software for popular Japanese, European, and American personal computers. Although it is not a smart card, in one version it can be programmed by a vending machine to dispense updated data-base information for display on either personal computers or on special portable readers having liquid-crystal displays.

Developed during a three-year effort by Mitsubishi Plastics Industries Ltd., the new card is an injection-molded slab of acryl-butadiene-styrene (ABS) 1.8 mm thick (a standard credit card is 0.8 mm thick). Inside is a single memory chip; it can be a mask read-only memory with up to 1-Mb capacity, a one-time electrically programmable ROM with up to 256-K capacity, or an electrically erasable programmable ROM with up to 256-K capacity. That makes the new card a strictly new medium, competitive with game cartridges and disks.

Volume market. Mitsubishi, now Japan's largest manufacturer of polyvinyl chloride sheets and films for credit cards, produced the new card as part of its search for new mass markets. About a year ago it signed up Hudson Soft Ltd., which claims to be Japan's largest game marketer, for the project.

The idea was to get a volume user of standardized software for the card. To promote the card's adoption as a standard, Mitsubishi will manufacture it and license its design to other makers.

Moreover, to ease multiple applications for programmable cards, a standard data format similar to that used on disks has been proposed. A committee of manufacturers and software houses has been convened by Mitsubishi to either ratify the tentative standard or develop a better one that all can agree to. (Data format for the games is predetermined by the machine in which they will be used.)

Play ball! The first product for the Japanese market will be a Hudson game called Baseball Craze, for MSX computers, scheduled to debut on the Japanese market this month with an initial production run of 20,000 cards (Hudson calls them "Bee" cards, after its trademark).

The price of the game card will be $19.20, a standard price for a game cartridge. An adapter to interface the cards with MSX computers will retail for just under $5. In the future, games will be available for popular Japanese computers and foreign makes such as Commodore 64 and the British makes Amstrad and Sinclair, according to Yuji Kudo, president of Hudson.

Tamotsu Koide, manager of the New Products Division at Mitsubishi, foresees a variety of applications in addition to games. One of the first will be storage of measurements of blood pressure and pulse, taken at home, which doctors can then use for patient diagnosis.

Checking blood pressure. Matsushita Electric Works Ltd. has made experimental automatic blood-pressure measuring systems that write on the cards and is working with several hospitals that may adopt this scheme. Data is read out and processed by personal computers. (Matsushita is an affiliate of Matsushita Electric Industrial Co, best known in the U.S. for its subsidiary, Panasonic Co.)

Cards with EEPROMs for downloading information from vending machines will have to wait until later this year or early next year. Hudson is having playback machines manufactured to its specifications and also plans to install a network of vending machines.

Chip-on-board packaging is used for

Gamesmanship. Japanese "Bee" card carries up to 1 Mb of mask ROM software for games. Cards with 256-K of EPROM or EEPROM for updated data-base applications are available.

the memory chip. The substrate is a 0.48-mm-thick glass-epoxy double-sided printed-circuit board with plated-through holes. The chip is die-bonded to the board; wire bonds are made between pads on chip and traces on board, and the chip encapsulated. Thirty-two metal-plated short plated traces on the back of the 25-mm by 51.2-mm board form an edge-card connector. The finished board mounts in a cavity at one end of the card. *–Charles L. Cohen*

MEDICAL ELECTRONICS

A WALKING SYSTEM FOR PARAPLEGICS GOES VLSI

Dayton, Ohio

Three years ago, a paraplegic Wright State University student named Nan Davis made international headlines when she took a few faltering steps thanks to computer-controlled electrical stimulation of her paralyzed legs.

The walking apparatus and closed-loop computer-control system, developed by Wright State University researcher Jerrold S. Petrofsky, has undergone significant refinement since then. Now Petrofsky is preparing to use the power of very large-scale integration to develop a miniaturized, self-contained controller that is the next step in pushing the experimental walking system toward commercial reality.

By summer's end, Petrofsky hopes to receive first working versions of a VLSI chip developed by NCR Corp. that will integrate most of the walking control functions on a single device. To be fabricated in low-power CMOS silicon-gate technology with features below 3 μm, the chip will mean a walking-control computer in a package about the size of a cigarette pack that can be worn on the belt of the disabled user.

Because of its low power—the device is expected to draw only about 1 to 3 mA at 5 V—the controller will require only a single, standard 9-V battery that will also be housed in the package. Eliminated will be the bulky, back-mounted battery pack used in current portable versions of the walking system.

All in one. The application-specific IC design will use NCR's semicustom macrocell technology to integrate a 65C02 microprocessor, various digital logic functions, a liquid-crystal-display driver, and 1-K byte of random-access memory on chip with 8-bit analog-to-digital and digital-to-analog converters. Also included will be from 8 to 20 stimulator channels by which the electrical pulses will be delivered to the user's leg muscles through electrodes contained in a so-called transcutaneous transducer garment developed by Bio-Stimu Trend Corp., Opa-locka, Fla.

Pulse stimulation in the closed-loop system will be directed based on input from sensors mounted on the user's hips, knees, ankles, and feet. Another key component is an orthotic brace developed at Louisiana State University.

Because of the high degree of integration on the controller chip, it will probably hit the maximum size—about 120,000 mil^2—that NCR can handle with its CMOS macrocell technology, says Richard L. Muterspaw, an applications engineer at NCR's Microelectronics Division in Miamisburg, Ohio. The digital portion of the chip, including RAM, will incorporate at least 24,000 transistors; the analog portions may take up to 40% of the real estate, Muterspaw says.

The controller IC will be fabricated at NCR's Fort Collins, Colo., facility. In the initial version, the control program will be housed in a separate programmable read-only memory IC, but later iterations using geometries of 1 μm or below will also integrate the program ROM as well as additional circuitry, and could be available next year, Muterspaw indicates. And Petrofsky is studying the possibility of implanting the controller circuitry in the user's body.

Big step. Jerrold S. Petrofsky will use a VLSI chip in a miniature version of the system he developed to help paraplegics walk.

A computer-controlled clinical exercise system based on a Wright State design for paraplegics, quadriplegics, and other disabled persons is already being marketed by Therapeutic Technologies Inc., Fort Lauderdale, Fla. An exercise system for home use as well as a hand-control system for quadriplegics have also received FDA approval and are expected to be commercially available soon, Petrofsky says.*–Wesley R. Iversen*

COMPANIES

JUNKINS HEADS TI AFTER BUCY SUDDENLY QUITS

Dallas

Texas Instruments Inc. shocked nearly everyone when it put out the word, just as the Memorial Day weekend was beginning, that J. Fred Bucy had suddenly resigned as president and chief executive officer. Equally surprising was that his successor was not a veteran of TI's semiconductor business, a major departure from the company's customary practice. The board elected Jerry R. Junkins as the new CEO, who, like Bucy, has spent his entire career with TI.

Bucy's sudden move came at a time when TI, particularly its chip business, had fallen on hard times. The Dallas company recently had to lay off thousands of its employees because of falling profits. His departure is expected to touch off a new round of reorganization at corporate levels this summer. When Bucy was elected CEO last year, it put him one step away from succeeding Mark Shepherd Jr., 62, as chairman.

The 56-year-old Bucy, who had served as TI president since 1976, opted for early retirement and plans "to pursue other interests," believed to be personal in nature. Bucy, on a sailing trip in the Gulf of Mexico, is unavailable for comment. However, it is known that the 32-year veteran of TI plans to remain as the senior adviser to the board.

As executive vice president, the 47-year-old Junkins was responsible for TI's activities in the government-equipment, computer, and industrial-controls markets. He is known for his manufacturing expertise and a "people-oriented management style," according to some TI managers. A year ago, he was elected to the board of directors, a step that made him a likely candidate for the presidency.

Nevertheless, Junkins was described by a company spokesman as being just as surprised as other TI managers were to learn of Bucy's decision, when the board quickly elected him president the

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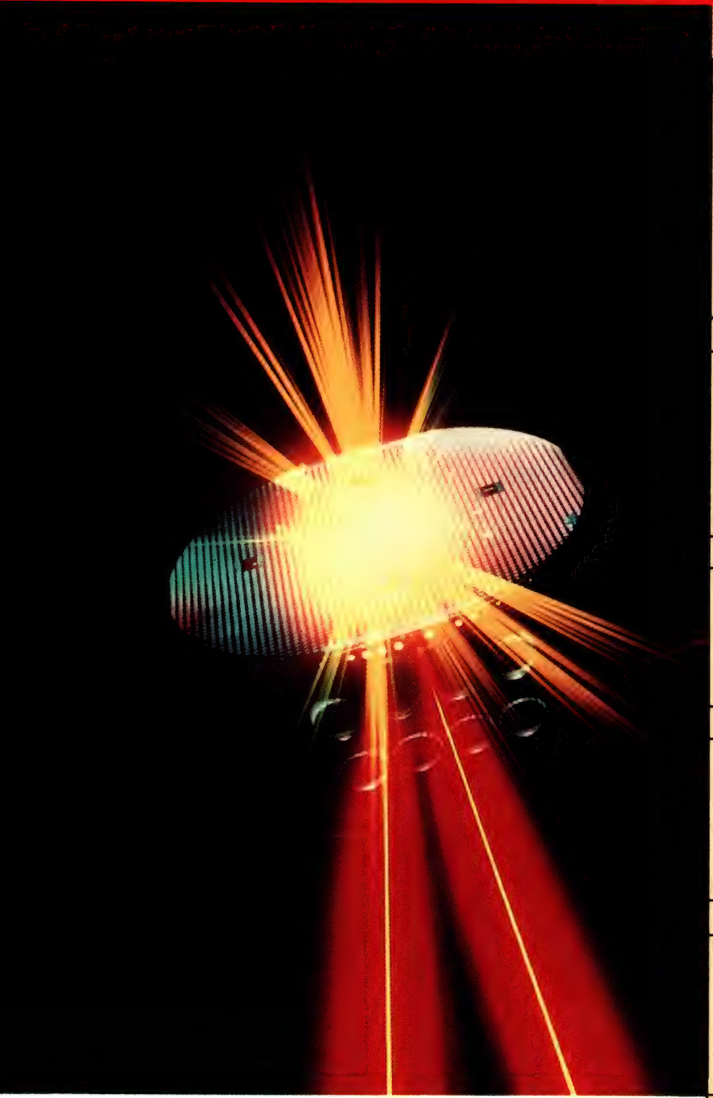

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HC/HCT193	Synchronous 4-Bit Binary Up/Down Counter
HC/HCT40102	8-Bit Synchronous BCD Down Counter
HC/HCT40103	8-Bit Binary Down Counter
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HC/HCT533*	Octal Transparent Latch; 3-State; Inverting
HC563*	Octal Transparent Latch; 3-State; Inverting
HC/HCT573*	Octal Transparent Latch; 3-State
DECODERS	
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HC/HCT138	3-to-8-Line Decoder/Demultiplexer; Inverting ✈
HC/HCT139	Dual 2-to-4-Line Decoder/Demultiplexer ✈
HC/HCT154	4-to-16-Line Decoder/Demultiplexer ✈
HC/HCT238	3-to-8-Line Decoder/Demultiplexer ✈
HC/HCT4514	4-to-16-Line Decoder/Demultiplexer with Input Latches
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HC/HCT245	Octal Bus Transceiver; 3-State ✈
HC/HCT640	Octal Bus Transceiver; 3-State; True/Inverting
HC/HCT643	Octal Bus Transceiver; 3-State; True/Inverting
HC/HCT646*	Octal Bus Transceiver/Register; 3-State
HC/HCT648	Octal Bus Transceiver/Register; 3-State; Inverting
ONE-SHOTS	
HC/HCT123	Dual Re-triggerable Monostable Multivibrator with Reset
HC/HCT221	Dual Monostable Multivibrator with Reset
HC/HCT423	Dual Re-triggerable Monostable Multivibrator with Reset
HC/HCT4538	Dual Precision Monostable Multivibrator
MISCELLANEOUS	
HC132	Quad 2-Input NAND Schmitt Trigger
HC/HCT280	8-Bit Odd/Even Parity Generator/Checker
HC/HCT670	4x4 Register File; 3-State
HC/HCT688	8-Bit Magnitude Comparator
HC/HCT4066	Quad Bilateral Switch

*Types with a bus driver output stage.

✈ Available in High-Rel types.

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HC/HCT02	Quad 2-Input NOR Gate	✈
HC/HCT08	Quad 2-Input AND Gate	✈
HC/HCT10	Triple 3-Input NAND Gate	✈
HC/HCT11	Triple 3-Input AND Gate	✈
HC/HCT20	Dual 4-Input NAND Gate	✈
HC/HCT27	Triple 3-Input NOR Gate	✈
HC/HCT30	8-Input NAND Gate	
HC/HCT32	Quad 2-Input OR Gate	✈
HC/HCT86	Quad 2-Input Exclusive OR Gate	✈
HC/HCT4075	Triple 3-Input OR Gate	

INVERTERS/BUFFERS/BUS DRIVERS

HC/HCT04	Hex Inverter; Buffered	✈
HCU04	Hex Inverter; Unbuffered	
HC/HCT240	Octal Buffer/Line Driver; 3-State; Inverting	
HC/HCT241	Octal Buffer/Line Driver; 3-State	
HC/HCT244	Octal Buffer/Line Driver; 3-State	✈
HC/HCT365*	Hex Buffer/Line Driver; 3-State	
HC/HCT366*	Hex Buffer/Line Driver; 3-State; Inverting	✈
HC/HCT367*	Hex Buffer/Line Driver; 3-State	✈
HC/HCT368*	Hex Buffer/Line Driver; 3-State; Inverting	✈
HC/HCT540	Octal Buffer/Line Driver; 3-State; Inverting	
HC/HCT541	Octal Buffer/Line Driver; 3-State	
HC4049	Hex Inverting HIGH-to-LOW Level Shifter	✈
HC4050	Hex HIGH-to-LOW Level Shifter	✈

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HC/HCT107	Dual J-K Flip-Flop with Reset	
HC/HCT109	Dual J-K Flip-Flop with Set and Reset	✈
HC/HCT173*	Quad D-Type Flip-Flop; 3-State	✈
HC/HCT174	Hex D-Type Flip-Flop with Reset	
HC/HCT175	Quad D-Type Flip-Flop with Reset	✈
HC/HCT273	Octal D-Type Flip-Flop with Reset	✈
HC/HCT374*	Octal D-Type Flip-Flop; 3-State	✈
HC/HCT377	Octal D-Type Flip-Flop with Data Enable	✈
HC/HCT534*	Octal D-Type Flip-Flop; 3-State; Inverting	
HC/HCT564*	Octal D-Type Flip-Flop; 3-State; Inverting	
HC/HCT574	Octal D-Type Flip-Flop; 3-State	

MULTIPLEXERS

HC/HCT151	8-Input Multiplexer	✈
HC/HCT157	Quad 2-Input Multiplexer	
HC/HCT158	Quad 2-Input Multiplexer; Inverting	✈
HC/HCT251	8-Input Multiplexer; 3-State	✈
HC/HCT253	Dual 4-Input Multiplexer; 3-State	✈
HC/HCT257*	Quad 2-Input Multiplexer; 3-State	✈
HC258	Quad 2-Line to 4-Line Data Selector/Multiplexer	
HC/HCT354	8-Input Multiplexer/Register; 3-State	
HC/HCT356	8-Input Multiplexer/Register; 3-State	
HC/HCT4052	Dual 4-Channel Analog Multiplexer/Demultiplexer	
HC/HCT4067	16-Channel Analog Multiplexer/Demultiplexer	

SHIFT REGISTERS

HC/HCT165	8-Bit Parallel-In/Serial-Out Shift Register	✈
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HC/HCT194	4-Bit Bidirectional Universal Shift Register	
HC/HCT195	4-Bit Parallel Access Shift Register	✈
HC/HCT299*	8-Bit Universal Shift Register; 3-State	✈
HCT4015	Dual 4-Bit Serial-In/Parallel-Out Shift Register	
HC/HCT40104*	4-Bit Bidirectional Universal Shift Register; 3-State	

Philips N.V. is an alternate source for RCA QMOS. Photo by Pete Turner, NYC.

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same day that it accepted Bucy's resignation.

"The world electronics industry is in a difficult period, which means real changes ahead," Junkins told TI workers in a memorandum circulated internally. He expressed confidence in TI's ability to overcome the soft demand for chips and computer products. This year, still-slumping semiconductor markets have been blamed for the tailspin of TI earnings.

Out. J. Fred Bucy has resigned as president of Texas Instruments Inc. after nine years in the job and 32 years with the company.

Immediately facing Junkins is the task of restructuring TI's five-member executive committee, which along with the new president and chairman Shepherd, charts corporate direction. Changes are expected in the management reporting structure of TI's Data Systems Group in Austin and the Equipment Group in Dallas.

But a company spokesman insists that the naming of a new president will not trigger sudden changes in strategies or the basic operational nature of TI. Many long-time company observers quickly note, however, that Junkins is the first TI president in nearly three decades without direct management experience in the firm's sprawling semiconductor products operations. As the executive vice president in charge of the Equipment Group, Junkins did have several dedicated semiconductor-fabrication front-ends under his control, including one for the Very High-Speed Integrated Circuits program and TI's gallium arsenide lines, which supply the needs of the firm's growing military-systems business.

Watchers of TI's corporate leadership now refocus their attention on Shepherd, who had been easing himself out of direct control of many operations. Shepherd, who reportedly clashed at times with Bucy over high-level product decisions, will probably take a more active role until Junkins becomes established.

–J. Robert Lineback

SEMICONDUCTORS

HITACHI SET TO RAMP UP 64-K BIPOLAR-CMOS CHIP

Tokyo

Semiconductor makers by and large are convinced that making memory chips is the best way to get the volume business essential for a payback on investments in advanced technology. And Hitachi Ltd. is demonstrating the conviction once again. The Tokyo firm is using a high-speed 64-K static random-access memory as the vehicle to bring its highly vaunted 2-μm Hi-BiCMOS (for bipolar CMOS) process on line [*Electronics-Week*, May 20, 1985, p. 13].

Hitachi is ramping up fast on the chip. True mass production in the range of a third to a half million parts per month is expected by early next year, a fast ramp-up for a new product. Initially, the price of the memory chips will be two or three times that of other 64-K SRAMs, but will eventually get down close to those of conventional chips.

Sales of Hi-BiCMOS gate arrays are expected to start sometime this summer, when designs of the various parts to be initially offered are completed; total volume of the gates, however, is expected to remain far below that of the memories because of the nature of the two businesses.

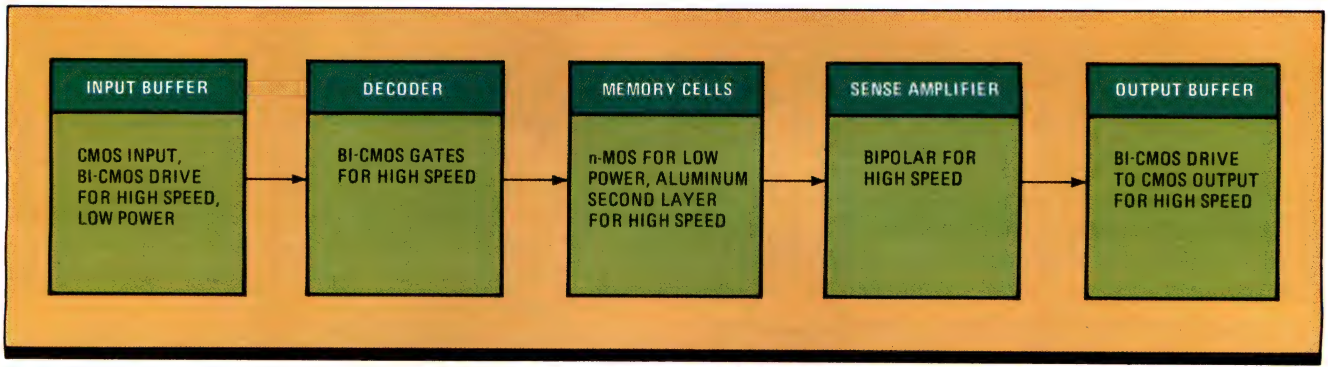
Applications for the SRAMs are expected to run the gamut of second-level cache memory in mainframes and superminicomputers with hierarchical memory schemes, main memory in supercomputers, fast graphics and picture memories, test- and measuring-equipment memory, and even future office-automation and personal computer functions.

Demand will be high, Hitachi figures, because nothing comparable exists. Bipolar devices with the same maximum access time of 25 ns are only available in capacities up to 16-K and require about three times the power, while CMOS memories with 64-K capacity are slightly more than half as fast: 45 ns maximum, compared with 25 ns. Also available are compromise CMOS parts with a capacity of 16-K and an access time of 35 ns.

Bipolar memories that are somewhat faster were announced at this year's International Solid State Circuits Conference [*ElectronicsWeek*, Feb. 11, 1985, p. 51], but they consume much more power and commercial versions may not actually be much faster than the 17-ns typical access time of the Hitachi devices. Fujitsu Ltd. announced a 10-ns offering and Fairchild Camera & Instrument Corp. a 15-ns part, but these most likely are performance records rather than typical data.

Surprisingly small. Despite the use of Hi-BiCMOS processing, the fast 64-K SRAMs are fabricated on an 8.5-by-3.4-mm chip barely larger than the current lower-speed 64-K CMOS SRAM. An important reason is that the memory cells, which take up the majority of the real estate, are almost identical with those used in earlier Hitachi CMOS SRAMs: four transistors and two high-resistance polysilicon load resistors. The same is true of the bonding pads, which account for much of the remaining space.

Hitachi engineers showed considerable flexibility when they designed the device, choosing not to stick slavishly


INPUT BUFFER
CMOS INPUT, BI-CMOS DRIVE FOR HIGH SPEED, LOW POWER
DECODER
BI-CMOS GATES FOR HIGH SPEED
MEMORY CELLS
n-MOS FOR LOW POWER, ALUMINUM SECOND LAYER FOR HIGH SPEED
SENSE AMPLIFIER
BIPOLAR FOR HIGH SPEED
OUTPUT BUFFER
BI-CMOS DRIVE TO CMOS OUTPUT FOR HIGH SPEED

Masterful mix. Instead of sticking slavishly to Hi-BiCMOS for their new 64-K SRAM, Hitachi designers used straight bipolar for the sense amplifiers, n-MOS for the memory cells, both CMOS and Hi-BiCMOS for the input and output buffers, and Hi-BiCMOS for the decoders.

with a purely Hi-BiCMOS approach. They used CMOS gates to improve speed when very low capacitance loads were involved, for example. The Hi-BiCMOS chip is faster, though, with moderately high capacitance loads.

For very top speed, Hitachi designed the sense amplifiers in straight bipolar technology. On the other hand, a CMOS output amplifier driven by Hi-BiCMOS drivers is used even though the MOS output transistors are large. This avoids special processing to reduce the effects of base saturation in bipolar devices, according to the firm.

Similar cells. In the final circuit configuration (see drawing), the input buffers have pure CMOS circuits followed by Hi-BiCMOS drivers for the decoders in order to achieve high speed at low power. The decoders are designed in Hi-BiCMOS for high speed.

As for the n-MOS memory cells, they are similar to those used for a number of years by Hitachi for low power, but have somewhat lower load resistors than used in devices designed for battery backup. Still, the load resistors are in the range from high megohms to low gigaohms. *–Charles L. Cohen*

CONVERTERS

PLESSEY SWITCHES OFF FLASH ADC, SAVES POWER

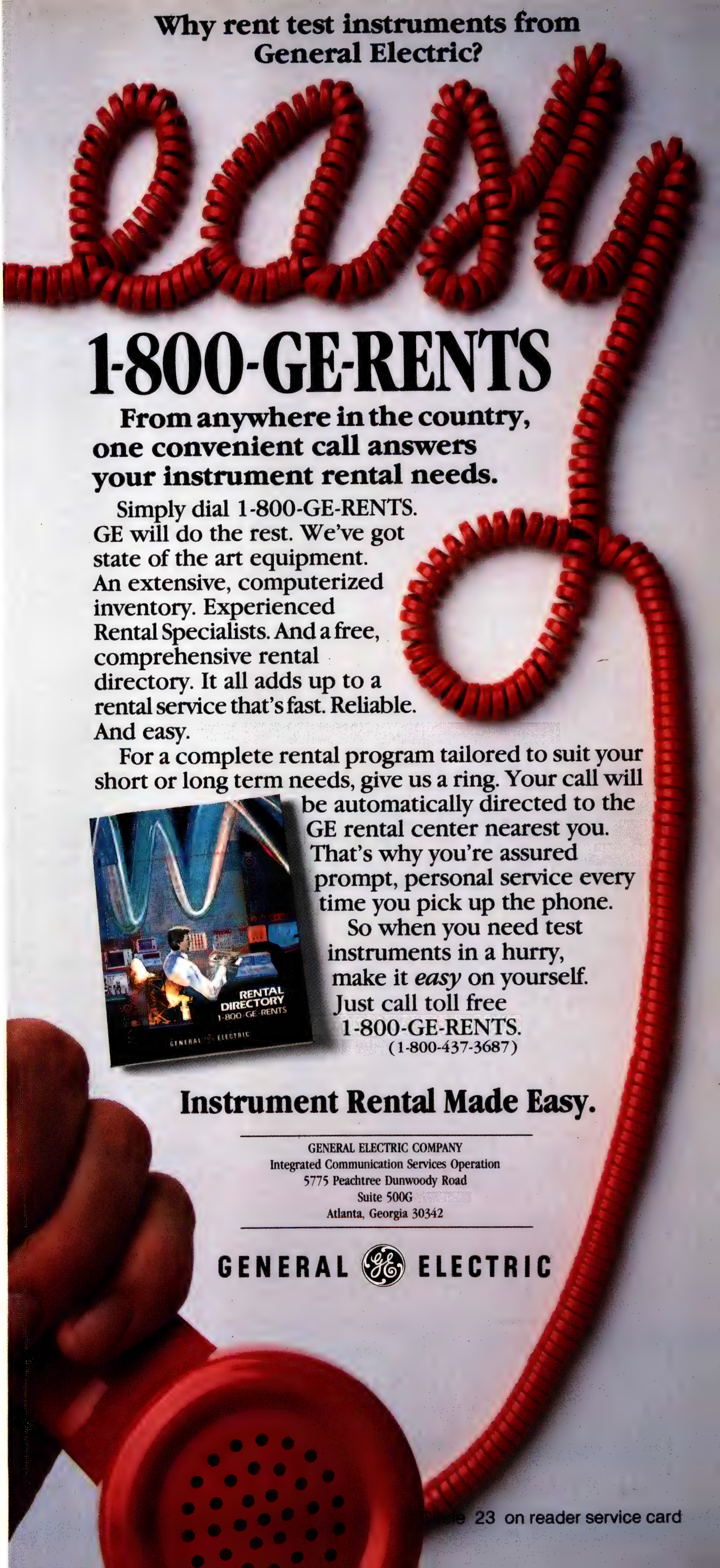
Caswell, UK

The flash, or all-parallel, analog-to-digital converter may be exceptionally fast, but it is expensive and power hungry. An experimental ADC now in development at Plessey Research (Caswell) Ltd. tackles both of these drawbacks.

In its high-performance ADC, Plessey's Converter Products Group uses a power-saving converter architecture that turns off unused circuit elements, together with a high-density bipolar process. The group is starting with an 8-bit part. The technique becomes increasingly attractive as more bits are added, and a 10-bit version will follow, says group leader Peter Saul.

These high-performance converters are slated for use in high-speed data links, digital video systems, radar, and other applications calling for fast conversion of analog signals. Setting the pace in the market now is TRW Inc.'s TDC 1007, which has a 30-MHz sampling rate and a power consumption of about 2.5 W.

Plessey's converter would be in direct competition with the TRW part. Though still in the lab, its specification looks attractive. A first-run chip operated at a sampling rate of more than 50 MHz con-



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sumed 1.6 W. Its analog bandwidth was 5 MHz, but Plessey says a modified version should be capable of the full 25-MHz Nyquist bandwidth.

Because flash converters simultaneously compare the incoming analog voltage with a set of reference voltages, each corresponding to a converter output value, the number of comparators doubles for every extra bit. Thus, an 8-bit model has 255 comparators. Yet in any sampling instant, the only comparators to generate useful information are the pair bracketing the analog signal. Where the reference voltage exceeds the input voltage, one of the two comparators will change from low to high output. The comparator outputs are encoded as desired.

Blocks of 16. In Plessey's new architecture, only those comparators close to the incoming signal are powered up. The chip's 255 comparators are sectioned into blocks of 16, each one of which can be individually powered up. This is done by a 4-bit preconverter, whose output switches on desired comparator blocks.

In theory, only one block at a time need be powered. But to gain speed, the converter operates in a free-running or unsampled mode, which means that the incoming signal could have a value falling midway between blocks. Comparator blocks also cannot be powered up instantaneously, thus the switching is arranged so that four comparator blocks are energized at any time. By energizing just 64 of the 255 comparators, only 1.6 W of power is used.

The converter seems more complex. But Plessey has designed simpler comparator blocks for an overall component saving: a single loading and latching stage is shared by four comparators, cutting the number of components for each set from 80 to 30. Because the precomparator adds components and the extra wiring takes up space, however, some of the component saving is lost.

The chip, which measures 4.2 by 4.5 mm, is made with a high-density oxide-isolated bipolar process with 3-μm features and two-layer metallization. Oxide isolation reduces transistor cell size by as much as 66% compared with its earlier 4-μm junction-isolated process, says Plessey.

Meanwhile, the move from that process's single-layer to double-layer metallization can cut chip area by 15%; three layers mean 25% less area. Three-layer metallization will be used to produce the 10-bit converter, says Saul. The converter was described at the seventh Custom Integrated Circuits Conference in Portland, Ore., last month. *–Kevin Smith*

PERSONAL COMPUTERS

OBJECT'S SHAPE DIGITIZED WITH HUMAN-LIKE METHOD

Toulouse, France

A small systems and software development company is about to go to market with a fast, cheap method of digitizing the shape of physical objects. Based on a clever data-acquisition scheme related to human vision, its developer, Eurosoft Informatique SA, expects it to have a broad range of applications, particularly in robotics and computer-aided design.

Eric Cosnard, product manager for the system, called 3-D Videolaser, claims that it has a considerable edge over existing schemes that are dedicated to the digitization and acquisition of shapes. "This is a very fast, precise, and automatic system and costs perhaps one-tenth the price of competitors based on, say, stereoscopy, ultrasonic waves, multiple-plane projection, and coded lighting," he asserts. "Mechanical probes might be somewhat more precise, but they are very slow and far from being automatic."

The hardware for the 3-D Videolaser consists of a 5-mW helium-neon laser, a turntable driven by a stepper motor, a standard video camera, an MS-DOS microcomputer manufactured by Y-E Data Inc. of Japan, and a data-acquisition and digitizing card manufactured by Eurosoft. The company chose the Japanese computer because when development of 3-D Videolaser began in 1981, it was the only machine offering a high-resolution (960 by 625 pixels) display. Eurosoft is currently developing a version of its system for use with the IBM Corp. Personal Computer/XT.

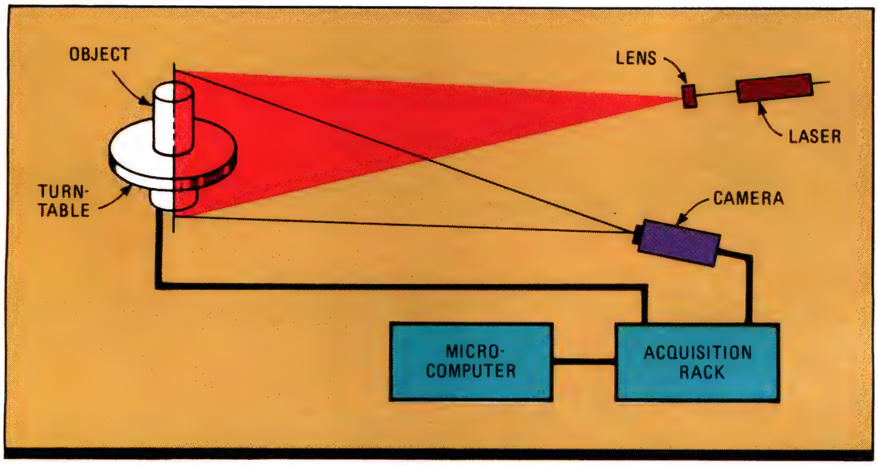
Plays its card. After a 15-minute calibration session, the object to be digitized is placed on the turntable where it is illuminated by the laser. Because the laser beam passes through a cylindrical lens, the light takes the form of a vertical plane. The video camera observes the scene from a fixed angle with reference to the plane of the light and passes the corresponding analog signal to the Eurosoft acquisition card.

The threshold of the card is set so that the part of the incoming video frame that was illuminated by the laser—a "meridian" of the object to be digitized—appears white, while the rest of the frame is black. The card receives lines from the camera at intervals of 64 μs and uses its 20-MHz clock as a reference to calculate the point(s) on each line that are white. This information is relayed to the microcomputer by means of a multibus interface, where it is recorded on a floppy disk.

This process is repeated at each step of the turntable, the system keeping track of which meridian it is recording with reference to the starting position of the turntable (for example, after the turntable has revolved 25% of a complete circle, the illuminated portion of the object is the 90° meridian). In this way, the 3-D Videolaser can plot some 200,000 points in less than 1 min with a theoretical resolution of 2×10^{-3}. The system software then filters the data and smooths meridians and parallels to present a relief image.

Cosnard says an important advantage of the system is its versatility. It can deal with any size object—on the condition that a suitable laser and turntable is available—without prior knowledge of the shape of the object. Many competing systems require such preprogramming, he says.

The obvious applications for the 3-D Videolaser are shape recognition in



Good shape. Eurosoft's 3-D Videolaser digitizes the shape of objects in less than 1 min. Software then filters the data and smooths meridians and parallels to present a relief image.

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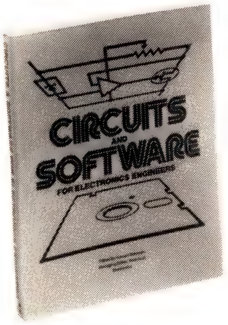

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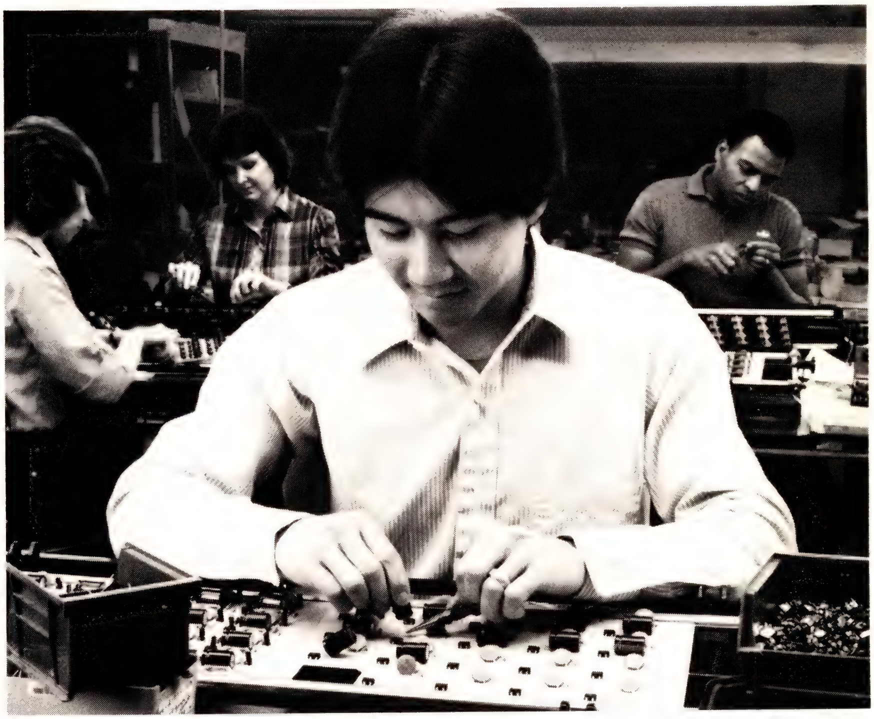

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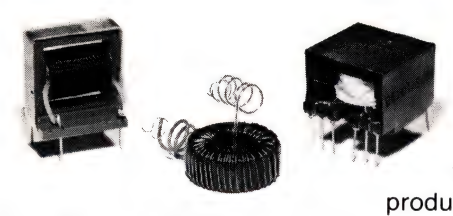

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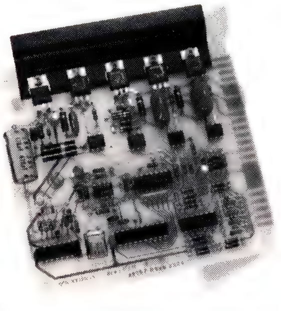

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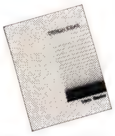

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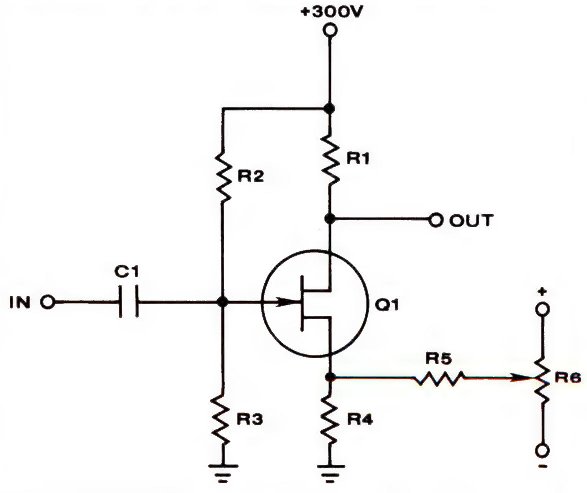

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robotics and automated production systems and modeling and alteration of existing objects using CAD systems. Other possible uses are in animation, data acquisition, and in the measurement of antique and fragile objects. *–Robert T. Gallagher*

PACKAGING

NEW APPROACH PROMISES GaAs INTERCONNECTIONS

Washington

A little-used layer-by-layer approach to building polyimide substrates may turn out to be the technology of choice for interconnections among gallium arsenide chips on a substrate, which will replace conventional strip-line packaging.

Building on earlier work using 5-mil (0.125-mm) lines and spacings in multilayer polymide substrates, a group at ITT Corp.'s Advanced Technology Center in Shelton, Conn., began three years ago to develop a five-layer substrate designed with buried, solid vias that serve as coaxial connections between chips. They now have achieved very-high-density interconnection for nine GaAs switching devices, each having 64 pins.

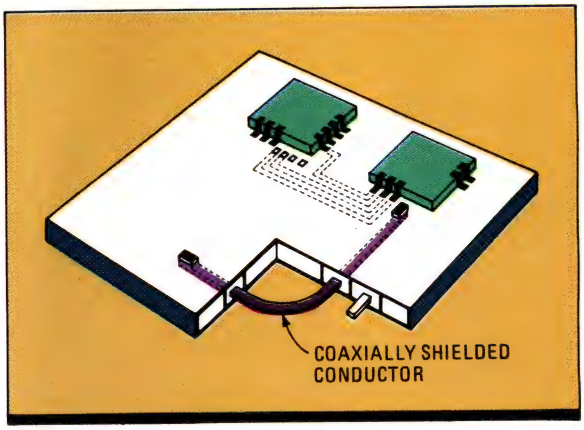
Speaking at the Electronic Components Conference here in late May, group leader Richard C. Landis, manager of advanced manufacturing technology at the center, characterized the buried connections as "a totally new technology for high-frequency circuits."

"Our goal is a point-to-point interconnect system," he told the meeting. The potential payoffs of such a system include reduced crosstalk between adjacent signal paths, good thermal characteristics, and fewer problems with increased impedance at high frequencies.

Buried conductors. Since GaAs systems are known to perform well in the range from 1 to 10 GHz, Landis's group, with the help of Augat Inc.'s Microtec Division in Newbury Park, Calif., fabricated a chip-to-chip interconnection with fully shielded coaxial conductors. Nine 64-pin large-scale-integrated devices with very high-density interconnections are bonded to surface pads on the substrate. The pads are then connected to 5-mil^2 solid vias within the 2-by-2-in. substrate that link the devices to the buried conductors (see figure).

Electrical test results for the technology with chips operating in the range from 1 to 10 GHz are promising. Using a special test fixture constructed to provide a contact between the test substrate and coaxial cable connections, Landis reports his group obtained a measured characteristic impedance of 52.3 Ω, slightly higher than his goal of 50 Ω.

Insertion losses from 1 to 10 GHz were less than 1 dB through 5 GHz and under 2 dB below 10 GHz. Return loss was reported well above 14 dB throughout the 1-to-5-GHz range. In addition, the fine-line polyimide substrate produced a 70% improvement in capacitance (at high densities) over ceramic thick film, Landis reports.



Buried coax. A fully shielded, curved coaxial conductor is buried within the multichip vehicle to reduce crosstalk and other problems associated with operating at high frequencies.

The packaging technology needed for the test substrate was developed at Augat Microtech (formerly Pactel Corp.) beginning in 1977. The layer-by-layer process uses electroplated-copper and solid-via (no plated holes) design. "We had a technology that was too early for the market," says Sanford Lebow, president of the Augat division.

Product needed. Lebow adds that Japanese firms have done similar work, but, until now, U.S. companies have essentially sat on the technology. "The next hurdle is for them [ITT] to design a product to use it in," he says. Lebow thinks the logical application would be in signal processing.

Landis says a second level of testing on more complicated chip-to-chip connections is needed before ITT will begin looking at product applications. "We hope to have our next round of tests completed by the end of the year."

Asked by ECC conferees about possible thermal-expansion problems, Landis conceded, "That's the next problem." Pressed for details, he claimed that "there is a simple solution to the problem" but declined to elaborate.

Landis predicts that the technology will have a significant effect on high-frequency packaging. "It's going to parallel the growth of gallium arsenide," he says, acknowledging that the semiconductor technology has so far been slow to develop. Further, he estimates that five-layer packages could be produced for less than $15 using a multiple-step fabrication process. *–George Leopold*

CONSUMER

SONY CAMPAIGNS HARD FOR 8-MM CAMCORDERS

Tokyo

Almost on the eve of this week's Consumer Electronics Show, Sony Corp. pulled out all the stops in its campaign to popularize 8-mm camcorders and video cassette recorders.

To inject new life into the 8-mm market, Sony president Norio Ohga unveiled not only seven new pieces of hardware but a new longer-playing tape (2 h instead of 1½ h) as well.

Sony made the biggest splash with an extremely compact single-unit record-only camcorder that can fit in an attaché case and weighs in at a mere 1.4 kg, loaded and ready to shoot (upper unit in photo, p. 30). It is paired with a portable playback machine (lower unit); and there are two full-size home decks that can play four hours using two-hour tapes.

When introducing the new gear last week, Ohga said, "We believe that the Mini-8 [Sony's tradename for the new 8-mm entries] is to video what the Sony Walkman personal stereo is to audio."

Producing a unit small enough to tuck into an attaché case "entailed a trick," Ohga admits. "The battery compartment with the grip and viewfinder can be detached, leaving a body that is only 55 mm thick." When set up for shooting, the camcorder measures 107 by 109 by 215 mm.

In the chips. Electronic-circuit packing density in the new camcorder is three times as high as its predecessor. Sony achieved the shrinkage by more intensive use of chip passive components, many mounted on ceramic hybrid integrated circuits. Moreover, circuits have been simplified and power drain reduced by designing the units for recording only. This added to the earlier savings in power achieved in the initial 8-mm product by switching to a charge-coupled-device imager in place of a conventional camera tube. A single battery charge provides 80 min of recording

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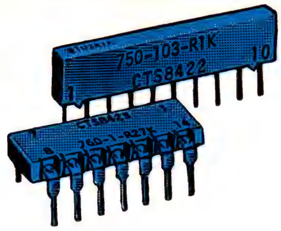

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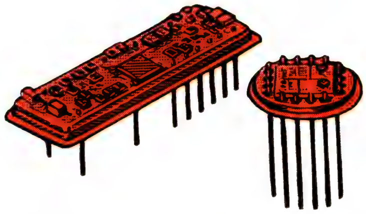

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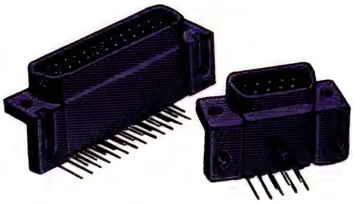

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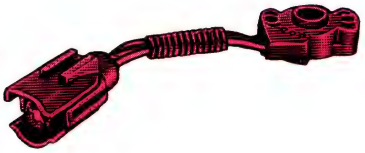

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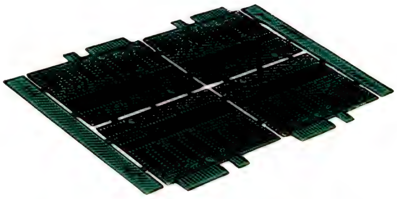

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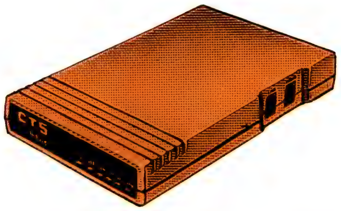

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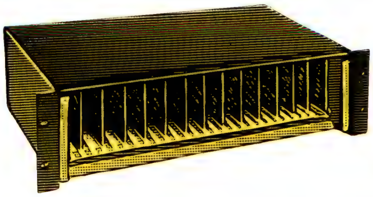

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On-the-go-video. Sony's 8mm camcorder (upper unit) will fit into a briefcase, and the company has high hopes it will do for video what its Walkman players did for audio.

time. Using a zone-focus lens of fixed focal length in place of the elaborate 6× zoom lens of the earlier camcorder further reduced size, weight, and cost.

The new 8mm camcorder will go on sale in Japan on Sept. 1 for $787, with an additional $588 for the portable deck. The price in the U.S. will be about $1,800 for both. Initial monthly production is slated for 20,000 units.

Standard tape VCRs were not forgotten, however; Sony is still working hard to hold on to its reduced market share. Ohga announced that all future Betamax VCRs would incorporate Sony's high-band technology for enhanced video quality. *–Charles L. Cohen*

LASERS

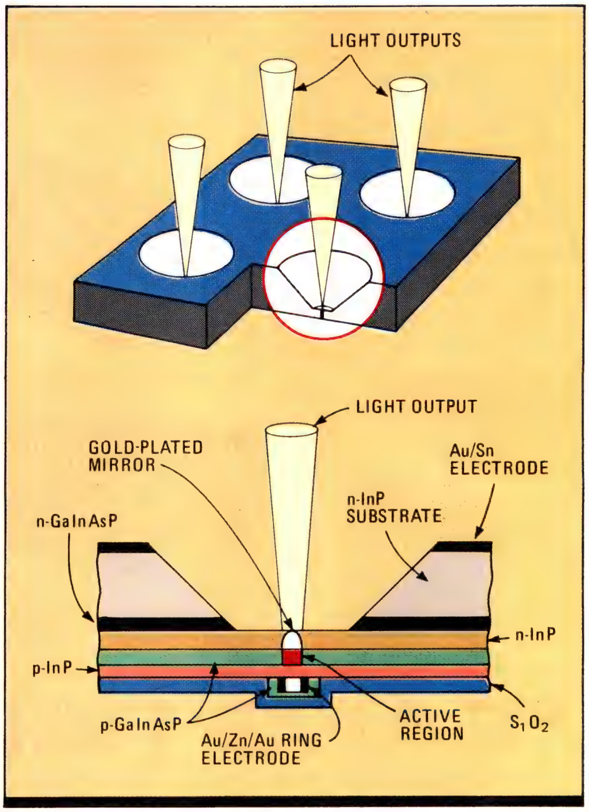
ARRAYS OF LASERS ARE BRIGHT SPOT AT CLEO

Baltimore

Twenty-five years ago, man created the laser. At the late-May Conference on Lasers and Electro-Optics here, which marked the silver anniversary of Theodore H. Maiman's first ruby laser experiment (see "Maiman sheds light on laser's history," p. 34), it was clear that the technology has gone forth and multiplied.

Some of the most interesting developments these days, in fact, are taking place right on the substrate. At CLEO, the word was arrays: multiple, low-power semiconductor lasers fabricated close together on a single substrate. Given the demand building up for modulators to drive fiber-optic trunk lines in long-distance telephone and data networks, laser arrays should wend their way rapidly from laboratories to piece-part production.

At CLEO, the Japanese showed that they have worked hard in this area. Most notably, Kenichi Iga of the Tokyo Institute of Technology, Yokohama, Japan, announced the development of a two-dimen-



Tight quarters. Angled mirrors are crucial to the tight packing of this GaInAsP laser array, developed at Japan's Tohoku University. The lasers, 30 μm in diameter, are spaced 1 mm apart.

sional laser array. Iga's group fabricated four lasers, each 30 μm in diameter and 1-μm high, spaced 1-mm apart on a single substrate of gallium indium arsenide phosphide (see drawing, p. 30).

This close-quarters construction breakthrough was made possible by a novel mirror design. In conventional lasers, mirrors must be etched perpendicular to the substrate's surface, straining the limits of current monolithic fabrication technology. Iga's array angles the mirrors at 45° instead.

This new array dovetails with recent highly touted work at Tohoku University in Sendai. There, in late April, a team headed by Humio Inaba announced that it had fabricated a 2-d array of 2,500 coaxial transverse-junction (CTJ) light-emitting diodes on a 5-mm by 5-mm chip. In these LEDs, the p-n junction is cylindrical and perpendicular to the substrate rather than parallel to it as in conventional LEDs. The transverse structure can have a longer active region than a parallel structure, and thus higher output.

At CLEO, Iga told *ElectronicsWeek* that his array, which lases, is a step ahead of the Tohoku group's array, which so far produces only incoherent light. (Inaba expects to obtain lasing by year end.)

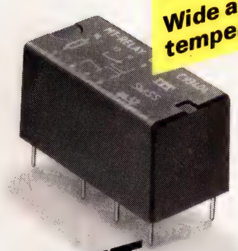
Iga notes that his device produces a relatively diffuse beam (9° in the far field), but believes advances in materials research—finding ways to hew thinner and smoother layers out of GaInAsP—will sharpen the output beam.

Improvements to the mirrors, which are fabricated without cleaving, should help up the output power from its current 1-mW ceiling. He sees potential use for the array as a modulator for telecommunications.

Combined beams. Other researchers have seen lasers in numbers—arrays—as the route to increased power. Chris Lindsay, a scientist at the California Institute of Technology, Pasadena, described a laser array that combines individual beams to generate a single higher-powered beam.

Developed along with Pam Derry and Ammon Yariv, the array aims to sidestep the problems typically encountered when high laser output is sought. That is, as input power rises to successive multiples of the laser's turn-on threshold, the output power of the laser beam also rises. However, beam spreading, or diffusion, occurs so that the light at the laser's target becomes a broadly focused cone. Thus, power per unit area at the target is not as high as desired.

To solve this problem, "We've ramped the gain slightly," says Lindsay. Caltech's phased-array semiconductor laser applies an assymetrical gain profile, by means of molecular-beam epitaxy, to a



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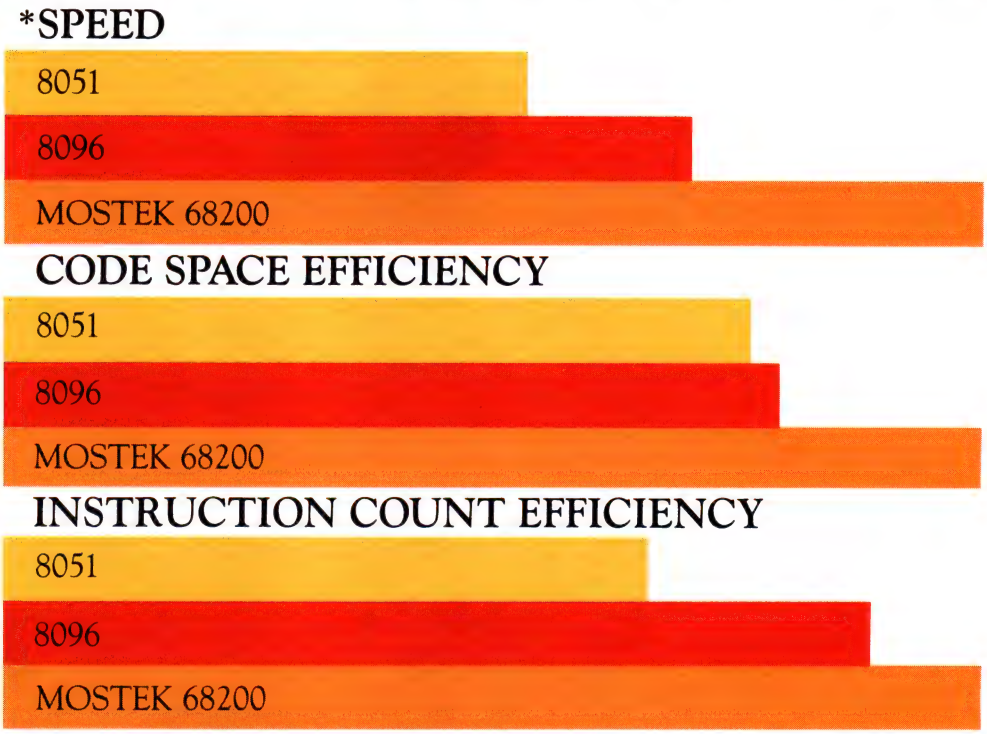

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row of lasers deposited on a single substrate. By tailoring the gain sensitivity versus the axis (angular direction) of emission for each laser, the demonstration unit was able to channel 200 mW of optical power into a 2°-wide beam and 450 mW into a 3.5° beam.

Another approach to achieving tightly focused output at power was described by Lew Goldberg of the Naval Research Laboratory, in Washington. In this method, injection locking, wherein a low-powered (4.8 mW) beam is pumped into the laser as a reference, was used. The technique was able to achieve a 105-mW continuous wave output in a 0.5° beam.

In pulsed operation, more relevant to real-world applications, 115 mW for 5-ns pulses and 43-mW 1- to 10-ns pulses were demonstrated. *–Alexander Wolfe*

MAIMAN SHEDS LIGHT ON LASER'S HISTORY

Of the seminal technological achievements that drive the electronics industry, none stirred such an initial soaring interest—and subsequent skepticism—as the laser. Only in recent years, in fact, has it become established as a virtually indispensable tool for science and industry.

No one has better credentials to put the laser's prospects into perspective than Theodore H. Maiman. On May 15, 1960, at Hughes Research Laboratories, in Malibu, Calif., he demonstrated the first working laser (Hughes announced it two months later). One year later, he left to organize one of the earliest laser companies.

Looking back, it is clear to Maiman, now 57, that a nearly universal "gee-whiz" reaction to the discovery escalated expectations to unrealistic levels. "What we had was a new kind of tool, but only experimental. People expected too much too soon," he adds. Further obscuring reality, even in those days before "Star Wars," was the science-fiction fascination with the laser as a possible "death-ray" weapon.

Unlike most other major technology advances, the laser had no immediate applications. The transistor, for example, was recognized at once as a replacement for vacuum tubes. The laser languished through most of the 1960s, a solution looking for problems. Another disappointment for Maiman was seeing a Nobel prize awarded in 1965 to a Columbia University physicist and two Russians who had developed the underlying theory for lasers.

But in the past few years, laser applications have taken off so that no accurate count of them is possible. In an advertisement scheduled to run nationwide July 15 to commemorate the laser, for example, Hughes Aircraft Co. cites 100 important uses.

Telecommunications use probably draws the most attention, partly because of the natural linkup between lasers and fiber optics. Slower to get going has been manufacturing, where the electronics industry has led the way. Here, the laser contributes to semiconductor production, slicing, dicing, annealing, and trimming. Still ahead lies a key role in building submicron devices, in Maiman's opinion, with an ultraoviolet laser that has already demonstrated it can trace circuit lines as small as 0.10 μm.

Yet Maiman's own interests now center on medicine, a field where laser applications continue to unfold. Since the first application took place in eye surgery—now a commonplace operation for repairing detached retinas—he has followed the ways doctors have employed his invention. At last week's CLEO conference, a full day was earmarked for papers on medical applications (see story p. 30).

The medical potential hit him dramatically at a convention in Cincinnati several years ago. There, a gastroenterologist demonstrated how a yttrium-aluminum-garnet laser operating through a fiber-optic probe could cauterize and stop extreme bleeding of a stomach ulcer. Through a beam splitter on the probe, he watched the 20-min procedure on a monitor. "This was an elderly woman, who couldn't undergo surgery, but she walked in and out of the office," he marvels.

Maiman now delves deeply into a wider range of applications, often consulting with hospitals. Already the laser medical tools are at hand. In addition to the YAG laser, whose speciality is penetrating tissue, the CO_2 laser serves as a scalpel, and an argon unit is used by ophthalmologists.

Other laser-based treatments show great promise. One of the newest is phototherapy, where a tracer element is injected in malignant cells, sensitizing them so that they can then be selectively killed by laser irradiation. Because of the growing range of light-irradiation treatments, Maiman believes there will be "a laser in every doctor's office within the next decade." **–Larry Waller**

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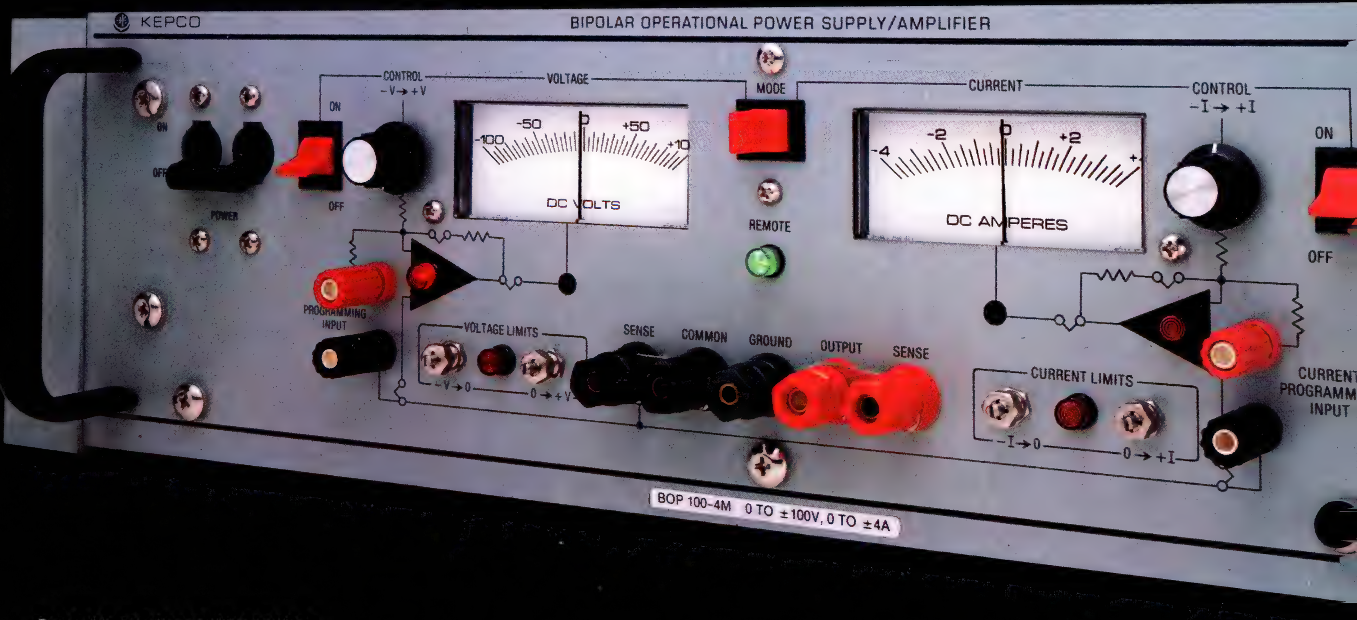

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TIME (8-hour drift):		<0.005%	0.01%	<0.01%	0.02%	<20µV	<1nA	<0.005%
TEMP., per °C:		<0.005%	0.01%	<0.01%	0.02%	<20µV	<1nA	<0.005%
RIPPLE and NOISE:(2)	rms	<1mV	3mV	<0.01%	0.03%	—	—	—
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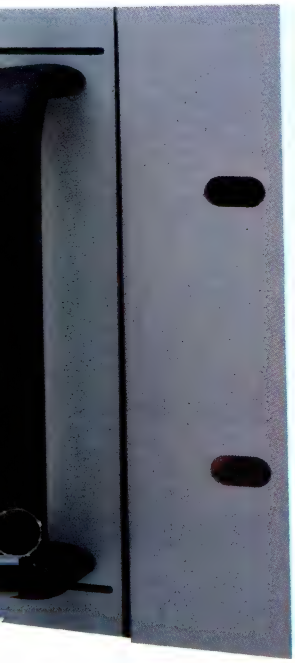
DYNAMIC SPECIFICATIONS

Parameter	Mode	BOP 20-10M	BOP 20-20M	BOP 36-6M	BOP 36-12M	BOP 50-2M	BOP 50-4M	BOP 50-8M	BOP 72-3M	BOP 72-6M	BOP 100-1M	BOP 100-2M	BOP 100-4M
Bandwidth (d-c to $f_{-3\,db}$)	V	3.0 kHz	2.0 kHz	1.8 kHz	2.8 kHz	4.5 kHz	2.8 kHz	3.3 kHz	2.0 kHz	2.0 kHz	4.0 kHz	3.0 kHz	2.0 kHz
	I	3.0 kHz	2.0 kHz	1.8 kHz	1.8 kHz	3.0 kHz	2.8 kHz	1.5 kHz	2.0 kHz	2.0 kHz	3.0 kHz	3.0 kHz	2.0 kHz
Programming Time Constant	V	50 µsec	80 µsec	85 µsec	55 µsec	35 µsec	55 µsec	50 µsec	80 µsec	80 µsec	40 µsec	50 µsec	80 µsec
	I	50 µsec	80 µsec	85 µsec	85 µsec	50 µsec	55 µsec	100 µsec	80 µsec	80 µsec	50 µsec	50 µsec	80 µsec
Large Signal Freq. Response	V	3.3 kHz	2.1 kHz	1.9 kHz	3.0 kHz	5.5 kHz	3.0 kHz	3.3 kHz	2.1 kHz	2.1 kHz	4.7 kHz	3.3 kHz	2.1 kHz
	I	3.1 kHz	2.1 kHz	1.9 kHz	1.9 kHz	3.1 kHz	3.0 kHz	1.5 kHz	2.1 kHz	2.1 kHz	3.5 kHz	3.3 kHz	2.1 kHz
Slewing Rate	V	0.4V/µsec	0.26V/µsec	0.4V/µsec	0.65V/µsec	1.7V/µsec	0.9V/µsec	1V/µsec	0.9V/µsec	0.9V/µsec	3V/µsec	2V/µsec	1.3V/µsec
	I	200 mA/µsec	260 mA/µsec	70 mA/µsec	140 mA/µsec	40 mA/µsec	75 mA/µsec	75 mA/µsec	40 mA/µsec	80 mA/µsec	22 mA/µsec	40 mA/µsec	50 mA/µsec
Recovery, Step Load	V	150 µsec	150 µsec	250 µsec	150 µsec	140 µsec	180 µsec	100 µsec	300 µsec	150 µsec	150 µsec	200 µsec	200 µsec
	I	30 µsec	50 µsec	30 µsec	30 µsec	30 µsec	30 µsec	50 µsec	30 µsec	50 µsec	40 µsec	30 µsec	50 µsec



	MODEL(1)	d-c OUTPUT RANGE E_O max.	I_O max.	CLOSED LOOP GAIN VOLTAGE CHANNEL G_V (V/V)	CURRENT CHANNEL G_I (A/V)	OUTPUT IMPEDANCE VOLTAGE MODE SERIES R	SERIES L	CURRENT MODE SHUNT R	SHUNT C
100 Watt	BOP 50-2M	± 50V	± 2A	5.0	0.2	0.5 mΩ	100µH	50 kΩ	0.05µF
	BOP 100-1M	±100V	± 1A	10.0	0.1	2.0 mΩ	200µH	100 kΩ	0.05µF
	Size: $5^{7}/_{32}$"H x $12^{17}/_{32}$"W x $17^{9}/_{64}$"D **Weight:** 48 lbs.								
200 Watt	BOP 20-10M	± 20V	±10A	2.0	1.0	40 µΩ	50µH	20 kΩ	0.1µF
	BOP 36-6M	± 36V	± 6A	3.6	0.6	120 µΩ	50µH	36 kΩ	0.1µF
	BOP 50-4M	± 50V	± 4A	5.0	0.4	0.25 mΩ	100µH	50 kΩ	0.05µF
	BOP 72-3M	± 72V	± 3A	7.2	0.3	0.48 mΩ	200µH	72 kΩ	0.05µF
	BOP 100-2M	±100V	± 2A	10.0	0.2	1.0 mΩ	200µH	100 kΩ	0.05µF
	Size: $5^{7}/_{32}$"H x $12^{17}/_{32}$"W x $17^{9}/_{64}$"D **Weight:** 51 lbs.								
400 Watt	BOP 20-20M	± 20V	±20A	2.0	2.0	20 µΩ	50µH	20 kΩ	0.2µF
	BOP 36-12M	± 36V	±12A	3.6	1.2	60 µΩ	50µH	36 kΩ	0.2µF
	BOP 50-8M	± 50V	± 8A	5.0	0.8	125 µΩ	100µH	50 kΩ	0.15µF
	BOP 72-6M	± 72V	± 6A	7.2	0.6	240 µΩ	200µH	72 kΩ	0.1µF
	BOP 100-4M	±100V	± 4A	10.0	0.4	500 µΩ	200µH	100 kΩ	0.1µF
	Size: $5^{7}/_{32}$"H x $16^{15}/_{32}$"W x $20^{5}/_{64}$"D **Weight:** 90 lbs.								

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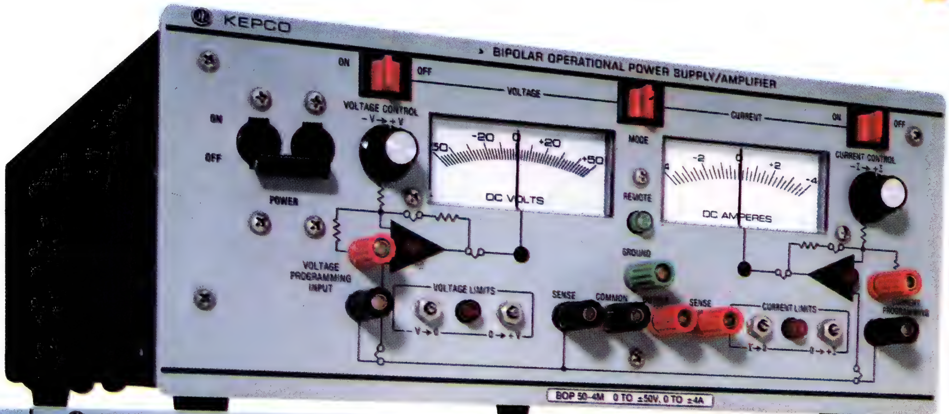
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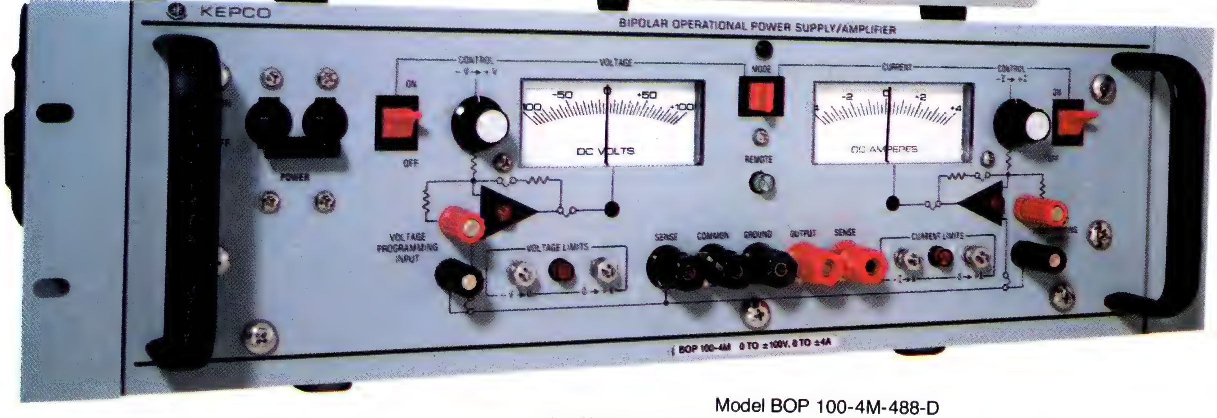
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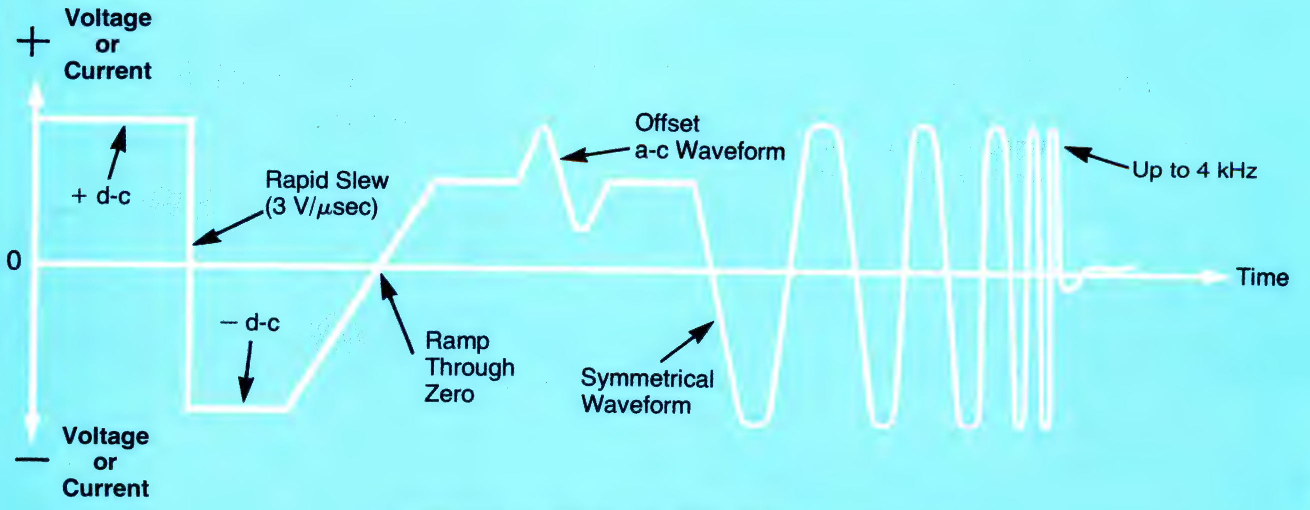

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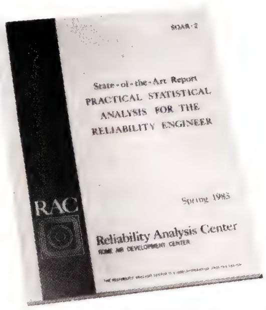

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FUZZY LOGIC PROVIDES NEW WAY TO DEAL WITH UNCERTAINTY

by John F. King

A NEW LOGIC SYSTEM HELPS COMPUTER SCIENTISTS DEAL WITH IMPRECISE PARAMETERS IN AI APPLICATIONS

New York

Ambiguities, those shades of gray that have always intrigued philosophers, poets, songwriters, and scientists, have no place in the Boolean logic that most computer architecture is based on. The Boolean world has no shades of gray: decisions are made by reducing elements to a series of black and white—yes or no—statements.

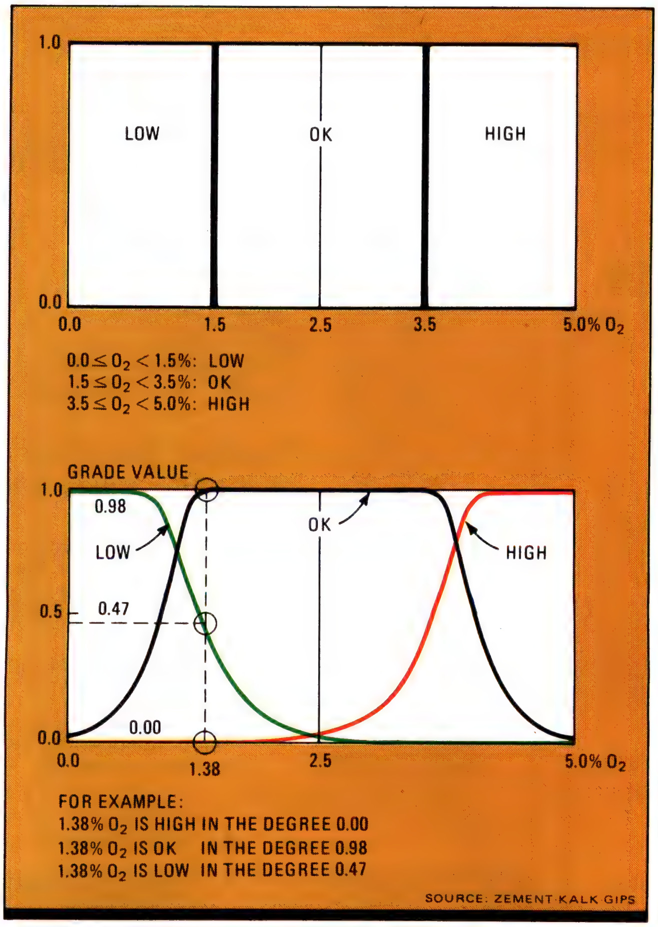
Computer scientists have thus far relied largely on probability theory to deal with the gray areas in applications such as expert systems, where statements can have varying degrees of truth. But a new way of dealing with uncertainty is gathering steam. That method goes by the oxymoronic yet appropriate name of fuzzy logic, the logic of approximate reasoning.

"Fuzzy logic is gaining by leaps and bounds," says James Besdick, president of the North American Fuzzy Information Processing Society. Applications in artificial intelligence and pattern recognition, which are "amenable to this type of thing," have caused this rapid growth, Besdick says. His group, founded just four years ago, has about 140 members and is one of five regional worldwide groups. The others are in China, India, Japan, and Europe.

This July, the first meeting of the International Fuzzy Systems Association—a separate worldwide organization—will take place in Palma, Majorca, Spain. Some 300 to 400 papers will be presented.

And last week, a design for an integrated circuit geared for processing fuzzy data was shown at the annual International Symposium on Multiple-Valued Logic at Queens University in Kingston, Ont., Canada, sponsored by the Institute of Electrical and Electronics Engineers. The IC was designed by Yamakawa Takeshi, an assistant professor of engineering at Kumamoto University in Tokyo.

Fuzzy logic has also attracted much interest, both in the scientific community and in the general press. Constantin Virgil Negoita of New York's Hunter College has published a book, *Expert Systems and Fuzzy Systems*, which describes Negoita's work in relating fuzzy logic with practical applications in AI. It is also selling briskly.



SOURCE: ZEMENT KALK GIPS

Graphic difference. The top graph uses classic true/false logic, the bottom graph, fuzzy logic. The bottom figure graphs low, okay, and high oxygen values. The intersection of a percentage with a curve tells to what precise degree the value is low, okay, or high.

But fuzzy logic remained obscure until recently. Its logic roots go back 20 years to the mathematical theory of fuzzy sets developed by Lofti Zadeh, now a professor of electrical engineering and computer science at the University of California at Berkeley.

Definitions. Zadeh defines a fuzzy set as "a class with unsharp boundaries." An example is the class of young adults. Standard logic would set sharp boundaries for such a set and give each set member an equal value. So, for example, in such a set every adult from 20 to 30 is equally young, but on one's 31st birthday, youth has vanished.

To accommodate the vague boundaries of such a class, a fuzzy set could define young adults as 15 to 35, for example. Values in the range of 0 to 1 are assigned to the members of that set. Thus, a member of 15 or a member of 35 could have a value of 0.1 membership in the set; a member of 17 or 33 could be 0.4, and members from 21 to 28 could have complete membership in the set (a value of 1.0).

Zadeh defines fuzzy logic as "the logic underlying approximate reasoning." And because "most of human reasoning is approximate reasoning," his system of logic provides a better model for human reasoning, he says. Besdick points out, however, that several systems are based on fuzzy sets, and users must pick the model that best suits the application.

An explanation of how a programmer can use fuzzy logic for approximate reasoning comes from Hans Berliner, senior research scientist in the computer science department of Pittsburgh's Carnegie-Mellon University. "Most complex decision making involves a series of approximations rather than one quick final decision," he says.

Berliner explains how this system works for the game-playing applications he designs. The programmer wants his logic model "to behave properly under a range of conditions. Standard logic allows you to say, 'if A is true, and B is true, then C.' In fuzzy logic, the value of C is a function of how true A is and how true B is. In this way, hundreds of variables can contribute."

The need for approximate reasoning applies especially to the development of expert systems. Ronald Yager, director of the Machine Intelligence Institute at Iona College in New Rochelle, N.Y., is developing an expert system shell called Fuzzexpert.

One problem in an expert system is how to represent human knowledge, he says. Despite its name, fuzzy logic is a "very precise way of representing imprecise information." Fuzzexpert allows the user to enter a set of data by drawing a curve on a graphics tablet. The curve corresponds to membership grades in the set. With Zadeh's logic system, the user can "turn verbal statements into formal statements" and "make the computer [the] servant rather than vice versa."

Minsky's view. Marvin Minsky of the Massachusetts Institute of Technology concedes that this logic system may be important, but says, "I find no need for it yet." In his view, fuzzy logic is an alternative to probability in dealing with uncertainty. He has heard users claim it is easier to make up membership numbers using it instead of probability.

Nonetheless, he's not particularly enamored of either system. "The way to deal with uncertainty is to make lists of reasons." Minsky offers the example of a set containing chairs, and says one should list the properties of a chair. Then when an attribute, such as length in a bench, doesn't match, "what you should say is it matches a chair in these respects but is longer."

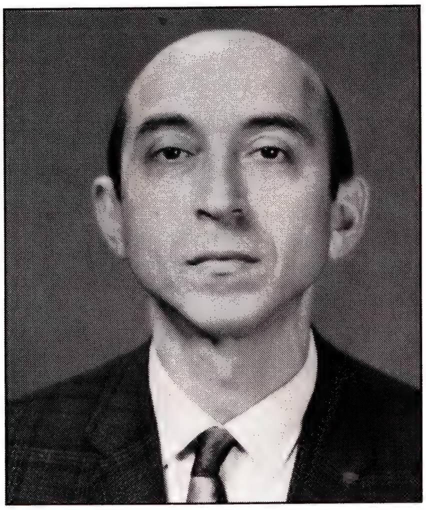
Compared with the theory of probability, though, Minsky says "the mathematics are just as neat. The theory isn't at all fuzzy." And the MIT professor says that in the long run, fuzzy logic may prove a "more natural" method than probability and equally useful.

Some of the earliest work in applying fuzzy logic to computer systems was done in West Germany at the Technical University of Aachen beginning in 1977. The team there, headed by Hans Zimmermann of the school's Department for Operations Research, has come up with two fuzzy models. One helps banks evaluate loan applicants; the other analyzes stock portfolios.

The eight-member team is thought to be the only group in Germany dedicated to fuzzy-logic work. It is now working on a fuzzy model to control production in flexible manufacturing setups. The model "weighs the various aspects and objectives against each other and seeks balances and compromises," explains Gerd-Wolfgang Hintz, a team member.

Besides those developed at Aachen, several software packages use fuzzy logic. A fuzzy-logic package called Reveal, for use in designing expert systems, was being sold in Britain by Tymshare (UK) Ltd., now a subsidiary of McDonnell Douglas Corp., before it was removed from the market for fine tuning. The original package, written by British consultant Peter Jones, served as a financial modeling tool. In late 1983, Tymshare rewrote the package as an expert system.

At the University of Vienna, Austria, a medical program called Cardiac-2 incorporates Zadeh's logic system and is helping doctors diagnose diseases. In Japan, Fuji Electric Co. of Tokyo recently announced development of a package for its L-300 personal computer that uses a fuzzy-logic approach to systems management. Fuji executives claim the package is a step more advanced than an expert system and leaves "fuzzy engineering" decisions to the computer.



Fuzzy logic founder. Lofti Zadeh, professor and electrical engineer, developed the twin concepts of fuzzy sets and fuzzy logic.

A recurring theme in fuzzy-logic applications is the idea of choosing a best alternative rather than narrowing options through straight logic until there is no choice. The need for flexibility in machine operation spurred the design of a cement-kiln controller at F.L. Smidth & Co. of Copenhagen, Denmark.

A human controller must weigh many factors and make variable judgments. Normal logic applied to automation of the process doesn't allow for the often vague degrees of precision, such as "rather high" and "reduce slightly." Beyond that, more than one rule for adjusting the mix could apply, and straight logic could dictate conflicting actions. Fuzzy-logic control attempts to simulate a skilled operator's running of the equipment, choosing the best applicable rule.

The control program defines terms such as high, low, normal, and okay (see figure). Quantities are then assigned exact values according to the degree of membership in the set for a term. Action is determined according to a weighted average of the range of actions that could be applied according to procedural rules.

Although Hitachi Ltd. of Tokyo avoids using the term fuzzy logic in its publicity for its automatic train operation (ATO) controller, similar principles are involved. In directing the starting, speed, and targeted stopping, the controller evaluates safety, riding comfort, energy saving, and running time, among other factors. It chooses a "most likely" control rule based on a human operator's experience. Plans call for the ATO controller to be ready for use on Tokyo subway systems in two years.

Fuzzy chip. Kumamoto University's Takeshi hopes to have a chip ready in two years. His chip design calls for a CMOS device of nine circuits, each of which will have grades of current from 0.0 to 1.0, with values that can match degrees of membership in a fuzzy set.

Takeshi thinks it may be possible to build a fuzzy computer, and he hopes to have a microprocessor ready within five years. He also says fuzzy-logic circuits will cost less to make than standard logic circuits. Such circuits would not need resistors, and Takeshi has a colorful explanation of other cost advantages.

"Most semicustom chips take time and lots of money to make. With fuzzy logic, you can mass-produce chips which will be capable of many sophisticated and specialized functions, at a cheaper price. It's like Cup o' Noodles, which you can buy cheaply, add all the condiments you want, and enjoy a dish at a fraction of the cost of going to a special noodle shop."

Whether or not fuzzy chips and computers ever become a reality, those working with Zadeh's logic system think it will affect the development of artificial intelligence in computers. Zadeh thinks that as people become more interested in developing expert systems for computer-aided design, they will gravitate to fuzzy logic. "Rules in expert systems are fuzzy rules, and most systems don't come to grips with that," he explains. Zadeh maintains that for now, expert systems can't handle the problem of managing uncertainty. ☐

Additional reporting was provided by Michael Berger, Jonathan Joseph, John Gosch, and Kevin Smith.

COMMERCIAL SPACE MARKET OF $47 BILLION PREDICTED BY 2000

by Alexander Wolfe

SMALL AND LARGE COMPANIES VIE FOR PLACES ON SHUTTLE, WITH SEMICONDUCTOR MATERIAL PROCESSING THE TOP VENTURE

New York

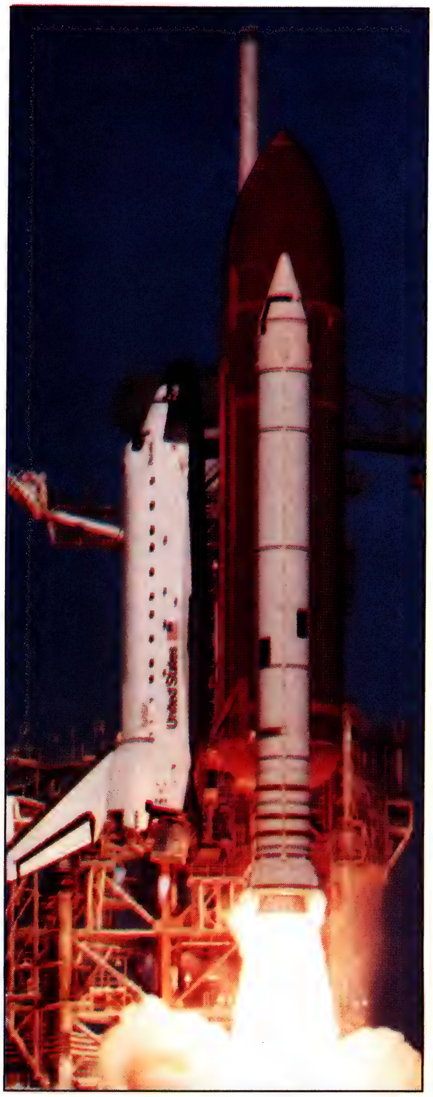
The economic colonization of space, spurred by the prospect of developing new and high-purity semiconductors and pharmaceuticals in a gravity-free environment, could produce $50 billion in commercial revenues by the year 2000, according to a soon-to-be released report. Today, space commercialization is being seeded by a host of startups, established firms, and the government.

The space shuttle has helped pave the way. Experiments have successfully run on the European-built Spacelab, a laboratory fitted into the shuttle's payload bay. And the U.S. space station, scheduled to be launched in the early 1990s, will incorporate a modified Spacelab for long-term use. This permanent orbiting scientific presence will mark the crossover point away from research and development dominated by a few individual companies to large-scale industrial participation in space commercialization, according to Mark Otterman, vice president of the Center for Space Policy. That Cambridge, Mass., forecasting firm wrote the report.

Although current federal budget-cutting may slow commercial development, space commercialization nevertheless has the force of government policy behind it. Indeed, on July 20, 1984, President Reagan proposed liberalized tax credits for companies investing in space R&D. The National Aeronautics and Space Administration began establishing commercial space-development centers to spread the gospel to industry and was allotted $30 million in fiscal 1986 to implement the policy.

Six segments. The new Center for Space Policy study predicts minimum and maximum gross annual revenues for the year 2000 (in 1984 dollars) for a commercial space marketplace divided into six major segments:

- Materials processing. Semiconductor and pharmaceutical production revenues will shoot from zero to somewhere between $2.8 billion and $20 billion.



- Space communications. Revenues of from $8.5 billion to $15.2 billion are expected for what is currently the most mature market segment.
- Remote sensing. The slowly emerging market for satellite data to aid mapping, agriculture, and geology should bring in between $500 million and $2.5 billion.
- On-orbit services. Running and maintaining the factories in space will gross from $300 million to $1.4 billion.
- Ground-support services. This segment will account for $5.9 billion to $10.2 billion, 90% of which is for satellite earth stations, the remainder for handling payloads before and launch and after landing.
- Commercial launch services. Non-NASA domestic rocket boosters (Ariane of France is a significant factor), have revenue-producing potential between $100 million and $700 million.

Crystal growth. Materials processing may hold the biggest long-term payoff. The prospect of growing gallium arsenide crystals in space has long been under study by NASA, in conjunction with producers of semiconductor materials [*Electronics*, Jan. 26, 1984, p. 89]. Space offers the prospect of greater purity and hence higher yield than is possible on earth.

It is the weightlessness of space that yields manifold fabrication advantages. In zero gravity, materials can be grown in containerless processors; because they don't touch a container's walls, they remain uncontaminated. Crystals can also be grown at lower temperatures than on earth, allowing for more stable structures. And, perhaps most importantly, materials of different weights that cannot be combined evenly under gravity can be alloyed in space, allowing development of new types of semiconductors, aerospace metals, and medicines.

Now, with R&D efforts under way on current shuttle missions, some companies are looking ahead to quick scale-up. "We will be able to produce commercial quantities on the shuttle itself," says Richard L. Randolph, president of Microgravity Research Associates Inc.

The Coral Gables, Fla., company is investing $25 million in its quest for space-grown GaAs crystals. Beginning in late 1986, experimental runs aboard the shuttle will use a miniature furnace. Eventually, Randolph hopes to produce up to 20 kg of GaAs crystal per flight. Later, he sees installation of a full-time factory on a space station in permanent orbit.

Louis Hemmerdinger, manager of space commercialization at Grumman Aerospace Corp., says that NASA will supply launch services and integration of Grumman's GaAs crystal-growth experiment. Grumman would build the crystal furnace and process the material. The company looks to a first flight in 1987, with six to eight experiments over three years. Currently, however, Grumman's interest is research.

For its part, Westech Systems Inc. believes that the quick road to commercial production may be lined with silicon. The company is ready to test its float-zone silicon crystal-growth experiment on the shuttle in late 1986. Because more baseline data is available on silicon than on GaAs, Westech thinks the space test will have a greater research benefit.

Test-flown on the Discovery last November, 3M Co.'s DMOS—for diffusive mixing of organic solutions—was the first project in a proposed 10-year program to investigate crystals of another kind. Urea crystals, with potential applications in fiber optics and pharmaceuticals, were grown; crystalline thin-film and organic polymer research will follow.

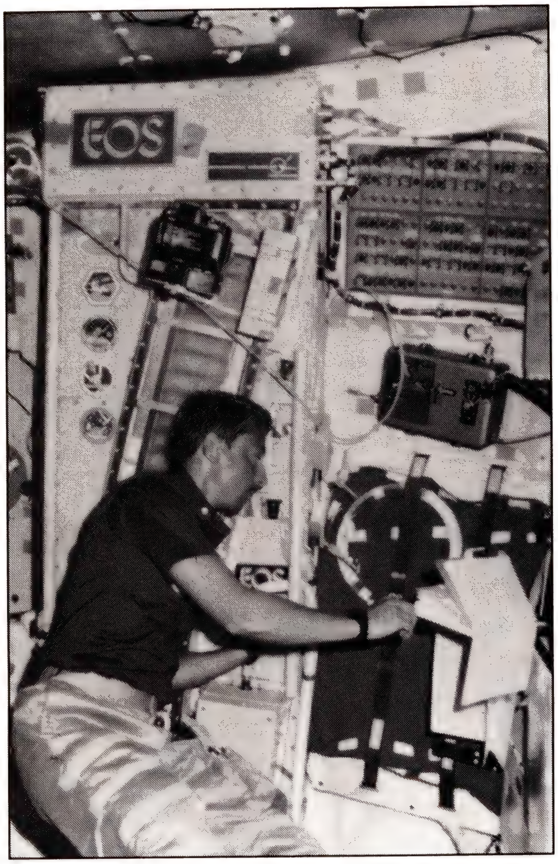
Although commercialization may proceed apace for companies currently signed on for the shuttle, that may not be the case for Johnny-come-latelies. Long lead times are the industry rule. The joint McDonnell Douglas Corp. and Johnson & Johnson electrophoresis experiments investigate separation of biological materials such as enzymes and hormones. The tests had been in the works for seven years before their first run on Discovery last August.

More significantly, millions must be invested in research and experimental shuttle flights before a payoff can be expected. And the goal—commercial production of crystals or medicines in space—is something that has never been done. Microgravity Technologies Inc., Solana Beach, Calif., projects a budget of $5 million to take it through eight to ten shuttle flights to its commercial milestone, production of a 100-kg GaAs crystal 4 to 6 in. in diameter. "I have run into difficulty raising funds because of the esoteric nature of the materials," says company president Bill Shelander.

To date, many private companies have been reluctant to get into space, he says. "Part of it is the perception that research in space costs many millions of dollars." Though his own budget bears this out, he notes, "We're trying to show that it can be done for a couple of hundred thousand per experiment."

Indeed, the drive toward cost-effectiveness has spawned a whole industry of space-service providers. They offer the full service spectrum from prelaunch and postflight payload processing, to boosters to thrust a satellite into orbit, right up to full-blown orbiting space stations housing crystal furnaces.

An entrepreneurial leader has been Orbital Sciences Corp. Founded in 1982 by three Harvard Business School graduates, the company develops upper-stage boosters. Its most recent product, the Transfer Orbit Stage, is a rocket that attaches to a payload and loads into the shuttle's cargo bay. Upon deployment from the shuttle, the TOS boosts the payload into its permanent high-altitude orbit. The unit cost about $50 million to develop, and will now be offered to commercial and government shuttle users for roughly $15 million per payload launch. General Dynamics and McDonnell Douglas Astronautics Co. also plan to offer upper-stage boosters.



Space walker. McDonnell Douglas's Charles D. Walker, aboard the shuttle Discovery, closes stowage area for biological samples supporting electrophoresis experiment.

The first privately owned payload-processing facility has been built in Florida near the Kennedy Space Center by Astrotech Space Operations Inc. The $7.5 million complex of three buildings boasts six environmentally controlled bays where satellites and experiment payloads can be serviced.

Private processing facilities in space—namely, non-NASA space stations—are actually orbiting labs for hire. Fairchild Industries is developing its $100 million Leasecraft platform, to be launched into orbit and periodically serviced by the shuttle. In the meantime, user equipment will churn away in space rented on the Leasecraft. Wyle Laboratories, Arlington, Va., is also developing a space lab for hire for the late 1990s.

Early birds. Historically, the first rental in space was space—that is, transponder space on a communications satellite. Long the only players in the commercial space field, satellites are already a mature market, with dozens in orbit.

One area that will drive future growth, however, is the bypass telecommunications market. AT&T Co.'s competitors, such as MCI Communications Inc., now offer an alternative to the Bell network for long-distance voice and data transmission. Demand for domestic services will increase demand for satellite transponder space, and thus for more satellites.

In addition, the administration is encouraging commercial competition with the Intelsat system. A global network (109 countries support Intelsat), these satellites serve U.S. companies by connecting them to Europe. Orion Satellite Corp., currently proposing two Ku-band satellites, is one of several new ventures seeking market share.

In addition to communications, a market is now seen for imaging, or remote-sensing, satellites. The satellite weather photograph has been a mainstay of the local news, but remote sensing for other applications has taken off less quickly than expected. Currently, the U.S. government operates the Landsat system.

Privatization of Landsat, as well as commercial growth of value-added services, is being encouraged. Transfer of the Landsat system to Eosat Corp., Arlington, Va., a joint venture of Hughes Aircraft Co. and RCA Corp.'s Astro Electronics Division, has been approved [*ElectronicsWeek*, May 27, 1985, p. 14]. ☐

SMART CARD FINALLY HITS U.S. SHORES IN TWO CITY TESTS

by Denise Caruso

CREDIT CARD WITH EMBEDDED MICROCOMPUTER WILL BE TRIED OUT BY MASTERCARD AS EXPERTS DEBATE ITS VIRTUES

San Francisco

The smart card has finally landed in America.

Five years ago, a group of entrepreneurs gathered at a conference in Columbus, Ohio, to explore that French invention—a microcomputer on a chip or two, embedded in plastic for use as a credit card. Next month, MasterCard will distribute smart cards bearing its logo to 100,000 consumers in Washington, D.C., and Florida, commencing a year-long trial to gauge consumer acceptance and viability for financial institutions.

Versions of the of the smart card already are being used with varying degrees of acceptance abroad, especially in France [*Electronics,* Jan. 26, 1984, p. 92]. Nevertheless, many observers believe that the U.S. trial is right on time—even though experts are still engaged in heated debate about such issues as applications and data security.

Skeptics abound. "As far as I can tell, it's still a technology looking for an application," says research analyst Anthea Stratigos of Dataquest Inc. "We've hardly even begun to look at it." Michael Burwen, president of the Palo Alto Management Group, agrees the smart-card market hasn't yet arrived. But he considered it important enough to form a separate division of his company, called Smart Card Reports, to track the market if and when it arrives.

Based on scenarios. "There's some potential, but it's all based on if-if-if scenarios," he declares. "So much depends on results of the different trials that are taking place." Although the company hasn't decided what market share smart-card technology will take, Burwen says it will probably share markets with both electronic-security and user-identification products. The market for security products, he estimates, will be $165 million in 1985 and will grow about 30% annually to $630 million in 1990. User identification devices will grow to $44 million in 1990, from this year's estimate of $33 million.

"Right now, smart cards' part of that is minuscule," he admits. "But, for example, if MasterCard likes the results of their trials, they've already said they'll adopt the technology. And they have 25 million cards out there right now. And if MasterCard adopts it, you know Visa won't be far behind."

Burwen explains that the success of the smart card, especially in financial applications, depends on the adoption of bioaccess, or biometric techniques for personal identification.

Biometrics (fingerprints, handprints, and the like) was one of the most hotly debated topics in San Francisco at the latest smart-card conference, which, like the first one, was sponsored by Battelle Columbus Laboratories. Many attendees, including Stratigos, were leery of the technology, although it is probably a major selling point for such vendors as banks who need assurance that people whom they provide with cash or goods are indeed who they say they are.

A credit card with a chip on board can help by performing its own off-line security checks. In addition to a customer-selected personal identification number (PIN), banks could store digital representations of their customers' fingerprints, eyeprints, signature dynamics, or handprints in the card's nonvolatile memory. Upon reading, if the proper biometric identification is not presented, cards may self-destruct or signal that a fraudulent transaction is in progress.

Problems galore. The smart card's problems range from insufficient memory—graphic representations can take up many thousands of bytes—to consumer acceptance. Although banks may like the high degree of security, others may

Card trick. Richard L. Dunham, president of Micro Card Technologies, with his company's card. Using the CP-8 chip from Motorola, it will be tested by MasterCard in Washington.

find it onerous. "The privacy of the person is a sacred cow," says Daniel Artusi, manager of strategic marketing for Motorola Inc.'s Semiconductor Product Sector in Phoenix, Ariz. The CP-8 chip that Motorola developed for Bull of France is being used by the company's Dallas subsidiary, Micro Card Technologies Inc., in the Washington MasterCard trial.

"Try to get an old lady from Oklahoma to use a card like that. Even signature dynamics I will approach carefully." Artusi says the cost of electronics for biometrics makes implementation impractical, not to mention that "we can't even agree on a national ID card using a fingerprint."

But the success of smart cards will have nothing to do with biometrics, Artusi claims. American standards organizations already are drafting protocol proposals for cards used in financial applications, and nonfinancial applications are multiplying.

Diverse applications. In addition to the highly publicized U.S. Army trial with datatags at Fort Benjamin Harrison in Indiana [*Electronics*, March 10, 1983, p. 52], smart-key products are also being used in vital medical applications such as kidney dialysis and the tracking of filtration systems for patients with artificial kidneys. Keys and smart cards are being used industrially as "set-up men" for assembly-line machinery and tasks such as auto painting. Some video companies are using keys to store special effects so that a given film clip will automatically be processed through a preprogrammed gyration.

Such independent uses need not come under the umbrella of standards organizations. But if the smart card is to be widely adopted for use by financial institutions and retailers, standards are essential—and much work has already been done to ensure uniformity throughout these industries.

Jerome Svigals, who was leader of the team that came up with the first magnetic-stripe card for IBM Corp., is an active proponent of smart-card standards. Author of *Smart Cards: The Ultimate Personal Computer* and a manager in IBM's Information Systems Group in Palo Alto, Svigals also is chairman of the committee on application and security architecture for banking systems that use ID cards and is well versed on the current status of how smart-card protocols are moving through the various committees.

The physical card standards for cross-industry financial transactions have been agreed on, he says. The International Organization for Standardization 97/17/4 protocol, which has been approved, states that such a card will look like a conventional credit card.

The question of where to put contacts is being voted on this week, says Svigals. The most likely position is below where the magnetic stripe is currently located and above the embossing.

"This is a major issue for the bankers," explains Svigals. "Since they don't want to have anything on the front of a card which interferes with their marketing logo." Also now in the works is an electronic signals protocol for voltage levels, frequencies, and sequences, which Svigals says should be available in draft form by year end.

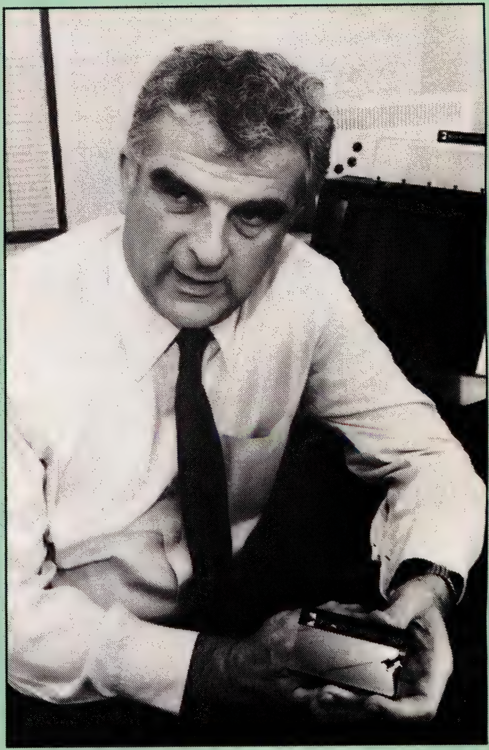
Perhaps most important, however, are standards that won't be in place for at least two years. ISO's TC68 committee, also the international committee for application and security architecture in the banking industry, has just started to meet. Svigals says it will take two to three years to draft proposals on these issues, and meanwhile vendors using smart cards can claim anything they want to about their system's security.

"Claims are being made by vendors, and there's been no independent verification of those claims," Svigals says about security issues. So he is pleased that part of the MasterCard trials will be an independent assessment of system security by Arthur D. Little & Co, the Cambridge, Mass., research firm. "I'm skeptical. I think some security is there, but it certainly needs testing. The timing is good." □

MEANWHILE, THE LASER CARD CRUISES ALONG

Uses for the laser-card technology developed by five-year-old Drexler Technology Corp. have been incubating for about as long as uses for the smart cards. Like Casio Microcard Corp. and MicroCard Technologies Inc., Drexler is getting its first crack at the open market. Recently, Blue Cross of Maryland announced it would use Drexler's Drexon laser card, with a storage capacity of 2 megabytes of information, for its Lifecard program.

Speculation has been rife for some time that Drexler, located in Mountain View, Calif., was having problems developing the read/write technology for the card, in which a laser bores 10-μm pits into a reflective surface very similar to that in laser disks. But founder Jerry Drexler (below) pooh-poohs the naysayers, mostly members of the smart-card industry, whom he calls purveyors of a "cute idea." Drexler was supposed to exhibit at recent Battelle conferences in San Francisco and Columbus, Ohio, but backed out at the last minute. That convinced those at the meetings that Drexler did not have the technology he had been promising since the company was founded. "They've been talking about it for years, but no one has seen [a reader/writer] yet," says one conference attendee who wished to remain nameless. Drexler says he just didn't want to pay the fee and that the smart-card people are just "chipping at [my] ankles."



But about the same time the conference was taking place in San Francisco, Drexler claims, the Stanford Research Institute completed its 32-month effort to develop a reader/writer for the Drexon card. He says the prototypes have just been shipped to Drexler licensees Canon, Matsushita, and Toshiba, who have paid \$200,000 to \$700,000 for access to the technology. Drexler has collected \$6.4 million from 20 licensees throughout the world, he says. In exchange, they build the readers or reader/writers for the card, write the specialized application software, and market the finished system, as well as buy the cards from Drexler. –D.C.

MARKET PRESSURES LEAD TO LEE DATA'S LOSSES

Once a major contender in the IBM 3270-compatible market, the young company lost $4.8 million in the last quarter

Minneapolis

Once a fast-rising star in the IBM 3270-compatible business, Lee Data Corp. last month reported a $4.8 million loss for its fourth quarter ending March 31. Those results included setting up a reserve for a $5 million bad debt incurred by Remington Rand Corp.—in which Lee Data holds a 19% stake—as well as other write-downs.

But the results indicate a trend and point up the rigors of life in the IBM Corp.-compatible business. The fourth quarter shortfall followed three consecutive quarters of declines and dragged year-end profits down to a measly $455,000 on sales of $91 million—compared with profits of $17.6 million on $98.7 million in revenues during the previous fiscal year.

Thanks to an innovative product line that anticipated IBM's moves in the 3270 data-entry terminal business [*Electronics*, Jan. 12, 1984, p. 109], by various estimates, Lee Data has snatched about 3% to 5% of a U.S. 3270-systems market that amounts to about $1 billion annually, with total market growth rates of approximately 15% a year.

But in recent years, IBM has moved aggressively into its 3270 marketplace, slashing prices and speeding up deliveries in its conventional terminals business, while adding features and announcing products aimed at bringing its PC line into the 3270 mainstream.

The IBM pressure has also taken its toll at other 3270-compatible vendors. Raytheon Co., for example, abandoned the market after heavy losses last year, selling its Raytheon Data Systems Division to Telex Corp., the leading 3270-compatible supplier. Though Telex saw record sales and earnings for its recently ended fiscal year, industry observers expect other casualties among weaker 3270-compatible makers.

Agility required. "IBM has demonstrated from a strategic, pricing, and delivery standpoint that it can move as fast or faster than any of the 3270-compatible vendors," observes Kenneth Bosomworth, president of International Resources Development Inc., a market-research firm. Bosomworth notes that future success for Lee Data as well as others in the 3270-compatible business will require a "great deal of agility" to counter expected continuing market moves by IBM. Typically, a young company such as Lee Data will "zoom up to $80 million to $100 million in sales, stagnate for a year, and then fall back," he warns.

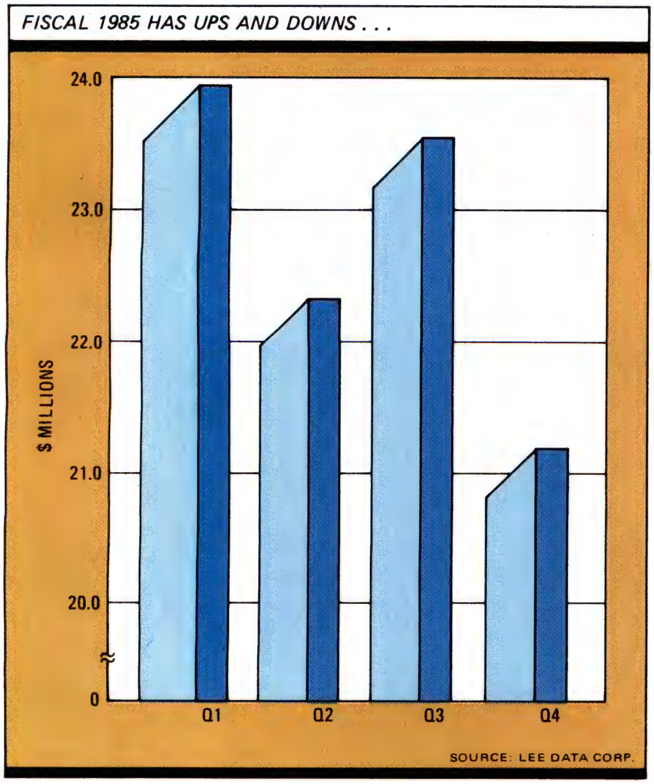
For his firm's part, chairman John M. Lee contends that Lee Data has the new products and plans necessary to turn its business around. First quarter sales in the current year will be higher than in any of the previous four quarters, Lee projects, because the firm has launched a cost-cutting program to improve product margins. Most visible was a 9% reduction in the work force in January; other plans are to begin cheaper offshore sourcing of components such as monitors and printed-circuit boards from Far Eastern producers.

Some observers think these moves are particularly important, because IBM's low-cost manufacturing capability will allow it to continue to put pressure on its smaller competitors' operating margins. Indeed, notes Frederic H. Sweeny, Lee Data's senior vice president for marketing, "We had 25% to 30% more product going out the door last year, but our revenues were 10% less because of IBM's price reductions."

TCP's success. One 3270-compatible supplier that apparently was not stung by tumbling margins last year was Telex Computer Products Inc. The Telex Corp. subsidiary saw its sales increase 113% during the fiscal year ended March 31 to $520.3 million, up from $243.9 million the previous year, while before-tax income jumped 70% from $53.5 million to $90.9 million last year.

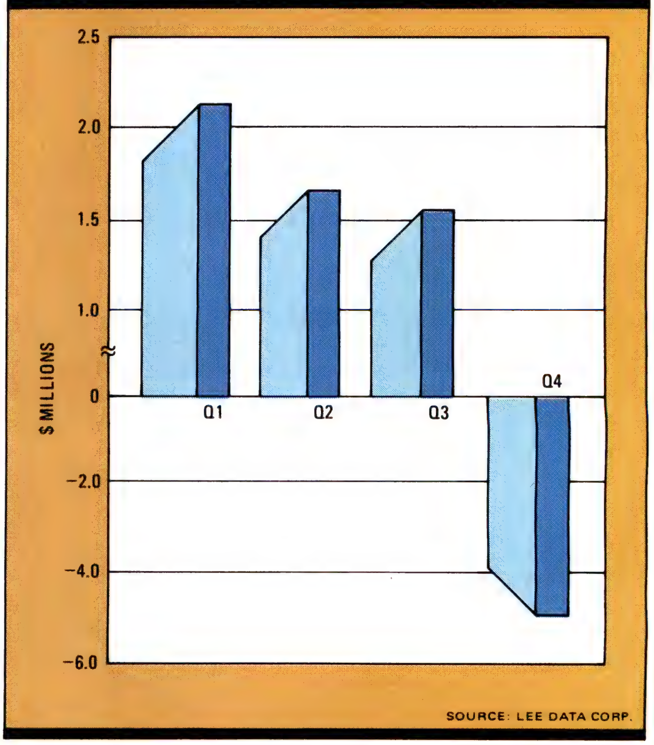
TCP now claims about a 14% share of

FISCAL 1985 HAS UPS AND DOWNS . . .



SOURCE: LEE DATA CORP.

. . . BUT PROFITS HAVE STEADILY FALLEN



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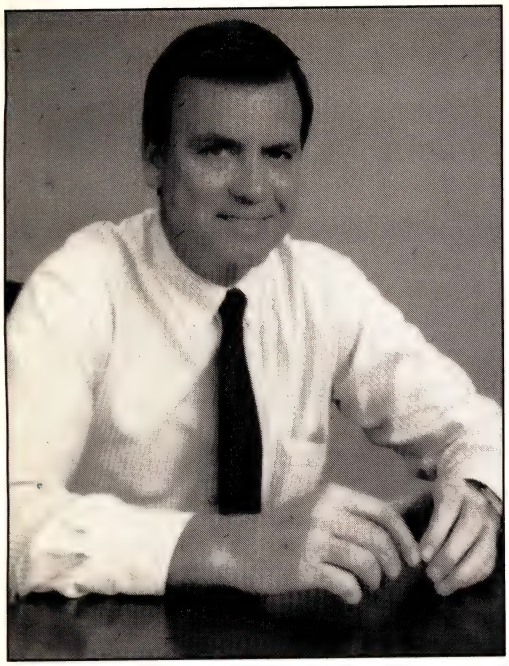


Diversify. John M. Lee, chairman of Lee Data, foresees a long-term need to diversify into other products.

the 3270 market, up from about 10 to 10.5% at the beginning of last year, says chairman and president George L. Bragg. About 3% of that gain in market share came from the Raytheon business, Bragg estimates. "I give Lee high marks for product creativity, but I don't think they've made the necessary investments to get their costs down."

Chairman Lee says his firm has also made "significant" investments in plant, with capital expenditures totaling about $27.3 million over the last three fiscal years. He notes that heavy automation investments aimed at reducing manufacturing costs might be more important to Telex, however, because "they build the same kind of product over and over."

Lee says, however, "our approach is to try to increase profitability by selling systems," with an emphasis on "unique product features" as opposed to competing against IBM directly on price. Because of that orientation, "our products include a lot more tailoring to the individual customer."

IBM's low-cost 3180 terminal introduced in March of last year, for example, includes the ability to handle interchangeably four different 3270 screen formats, matching a similar capability in Lee Data's All-in-One 1221 terminal, priced at $2,066 and released in 1981. In a similar way, IBM's 3270 Personal Computer introduced in October 1983 [*Electronics*, Nov. 3, 1983, p. 47], erased a previous Lee Data product advantage by offering personal computer and data-entry terminal functionality in the same machine. IBM turned the screws last summer by adding two new 3270 PC models and host software that provide advanced graphics capabilities.

"Historically, when IBM introduces new products, they typically gain market share in the early years, and then the independents come back and begin taking share from them. It's a cycle that repeats itself every four or five years," says Lee. "We're at the point now where our response products [to recent IBM introductions] are out and have been shipping for four of five months, and we believe we have our advantage back."

That perceived advantage is riding partly on the strength of Lee Data's 1221-W, a $2,866 version of its All-in-One terminal that provides a software windowing so that data from up to four separate hosts can be accessed simultaneously. IBM currently provides this feature only on the 3270 PC, which sells for about twice the price of the new Lee Data display. When used with Lee Data's 400 series controllers, the 1221-W also can process data in separate windows from asynchronous non-IBM hosts and from IBM mainframes, Sweeny says.

Lee Data also looks to its Series 70 Personal Workstation announced last summer and now on sale to begin boosting sales soon. Lee says its Series 70 provides color graphics, seven software windows, and other features matching those of the PC 3270 while incorporating dual microprocessors.

Despite the optimism voiced by officials at the Minneapolis firm, some industry watchers aren't so sure that Lee Data's unique-features strategy will continue to carry the company. "I don't think they've fully regained the market uniqueness they had," says Gary P. Smaby, vice president and senior technology analyst at Piper Jaffray & Hopwood Inc., a Minneapolis investment firm. "Because of the way the dynamics of the market have changed, it will be much more difficult for them to enjoy the kind of growth they've seen in the past because of that strategy."

Focus on niches. IBM could easily match the features of the 1221-W and Series 70 models if it chooses, Smaby points out. Given IBM's recent broad attack on the business and a general maturing of the 3270 market, Smaby figures Lee Data will be forced to focus more on market niches.

"They really had a nice umbrella to work under in the early years when they were selling virtually across IBM's marketplace, but that umbrella now has shrunk," Smaby says of Lee Data's strategy. He adds that the firm will still grow, but at a more moderate rate than in the past. *–Wesley R. Iversen*

BOTTOM LINES

HP speaks out on new projects

Hewlett-Packard Co. at a meeting for security analysts in New York on May 21 announced a new computer-integrated-manufacturing push and updated news about Spectrum, HP's project to convert its entire hardware line to the reduced-instruction-set-computer concept [*ElectronicsWeek*, April 29, 1985, p. 36]. On the first point, HP said it will offer its CIM expertise to any company where an electronics part is a primary component of the end product. Such a market includes companies in the automotive and appliance industries, and HP officials estimate this as a potential market of $5 billion to $6 billion. Spectrum is on schedule with a major announcement to come by the end of the year, according to the Palo Alto firm, although no product shipments will occur in 1985. HP is now in the process of testing more than 100 prototype systems.

Quantum leaps in sales

Quantum Corp. of Milpitas, Calif., a leading maker of Winchester disk drives, announced a 79% increase in sales for the fiscal year ending March 31. Net income for the year jumped 97% to almost $21 million from approximately $10.7 million for the past fiscal year. Quantum president James L. Patterson attributes the sales increase to the success of the Q500 5¼-in. Winchester drive product family as well as to a continuing strong demand for the Q2000 8-in. Winchester products.

Fibronics splits stock

On May 20, Fibronics International Inc., a fiber-optics communications firm, announced a three-for-two stock split. Each stockholder of record on May 31 will receive one additional share for each two held, to be distributed on June 12. The company will pay cash in lieu of fractional shares. J. Morris Weinberg, chairman of the board for the Hyannis, Mass., firm, says the 50% dividend results from "consistent interest in Fibronics on the part of investors" which "has made it advantageous to broaden the number of shares available for trading."

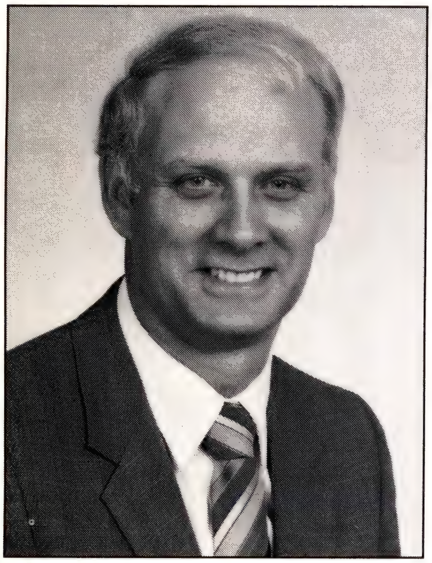
Second round for Scientific

Now in the process of building a computer system compatible with the Cray XMP series and aimed at large-scale engineering and scientific markets, Scientific Computer Systems Corp. of Wilsonville, Ore., recently secured second-round financing of $15 million. This round brings the company's total venture financing to $17.7 million, and it expects to be making its first customer shipments in the spring of 1986.

ELSON HEADS GM MOVE TO PUSH MACHINE VISION

Warren, Mich.

Gerald L. Elson sees plenty of machine vision in General Motors Corp.'s future. Elson, 43, was named full-time executive director of GM's Machine Intelligence Technology Implementation Section last August, when GM acquired equity stakes in three machine-vision companies [*ElectronicsWeek*, Aug. 13, 1984, p. 11].



Implementer. GM machine-vision director Gerald Elson is eager to see the technology find widespread use on the factory floor.

Elson had a hand in the original three equity purchases and has since helped set up similar deals involving GM stakes in two additional machine-vision makers. "What we don't want to happen is to have the implementation time [for machine-vision systems] strung out like it was with robotics," he declares.

A GM career man, Elson has held several management and supervisory positions, including a stint from 1980 to 1982 as a plant manager for General Motors Ltd. of London. Just prior to his new position, he headed GM's Manufacturing Systems Group, which covers robotics, industrial engineering development, computer-aided control systems, and planning and scheduling systems, as well as machine vision.

Billion-dollar stake. Recent internal surveys have identified a need for at least 44,000 vision systems in GM plants by 1990, up from fewer than 500 systems in use today. If that goal is met, machine vision at GM will be more pervasive than robots—which are expected to number about 14,000 at the firm by decade's end—and GM's investment in vision will total well over $1 billion.

Elson sees the entire machine-intelligence activity, which includes factory application of artificial-intelligence systems as well as vision, as vital to GM's future. "I just feel that this is a technology that has got to be developed and utilized if we are going to become competitive in the automotive manufacturing market in North America."

If GM is to meet its ambitious machine-vision goals, several things have to happen, says Elson. "We have to have some breakthroughs in the technology. Speed and reliability have to go up, and the cost has to come down." In addition, he says vision systems must become more generic so they can be applied across large classes of problems at a variety of GM plants.

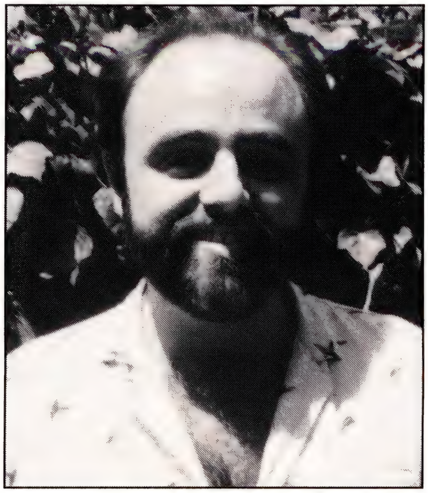
"We really have to get into some high-volume applications," Elson observes. "Everything right now is too tailored to a 'one-off' situation, and I think that's really hurting the industry."

Elson thinks another problem lies in adequately training enough applications engineers in the use and maintenance of the equipment on the factory floor. To help meet its own massive training needs, GM is developing internal training programs. *–Wesley R. Iversen*

POET NEWMAN CAPTURES THE MUSE IN PROGRAM FORM

Palo Alto

Michael J. Newman defies those who believe programming and poetry don't mix. A poet with a bent for computing and biology, he has dedicated himself to the task of translating poetic forms into the electronic medium. By blending educational and entertainment aspects into software, Newman believes he has developed a product of a new genre, a "full-blown creative utility."



The fruit of his efforts with partner and fellow interdisciplinarian Hillel Chiel, a postdoctoral student in neurobiology and behavior who also holds a BA in literature, and programmer Paul Holzer is called the Poetry Processor. Running on an IBM Corp. Personal Computer, the program consists of three main elements. A spreadsheet demonstrates poetic forms by highlighting rhyming words with up to 12 colors and sounding out tones to demonstrate rhythm. A text editor outlines the user's choice of poem, such as a sonnet, and provides access to a rhyming dictionary. And relational data bases contain 400 of Newman's poems and the user's own.

Newman, 38, previously designed tutorial board games and several as-yet-unsold computer games geared for teaching biology principles to children. Last year, he and his colleagues changed their focus when Newman decided his Poetry Processor had a better chance to sell than his biology games.

Although he hasn't yet sold any copies, Newman is working with a software agent, and some educators have embraced the program. On May 1, for example, it was used to instruct a class at Stanford University in poetic forms.

Appropriate. One reason Newman thinks the program could become popular is that it will be one of the few programs that deals seriously with language. "Language is handled so trivially in the [educational software] business now. They make the subject matter simplistic, and that's dumb. They should make it teach powerful material and languages," he believes. With his program, he says "there is appropriateness of the medium for the content—that's what makes a difference."

Newman also believes that a large number of people will be drawn, as he is, into the game-like nature of fitting words to a specific poetic form. The program starts with an uncompleted poem and prompts users to "clone poems." One of his specialties as a poet is in fact cloning the work of great poets by matching their form and general content but changing some of the words.

If successful, Newman would like to add an Instant Anthology feature to let sonnet-hackers send their poems by modem and trade text changes with each other through a special service on a local-area network. *–Eve Bennett*

Poet programmer. Michael J. Newman has developed a program called Poetry Processor, which teaches poetic forms.

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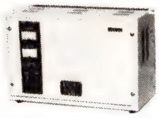
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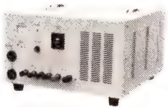
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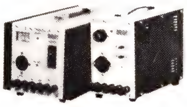
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Freq. Stability	50/60Hz ±1Hz max.			50/60 & 400Hz ±f × 10⁻⁴max.		
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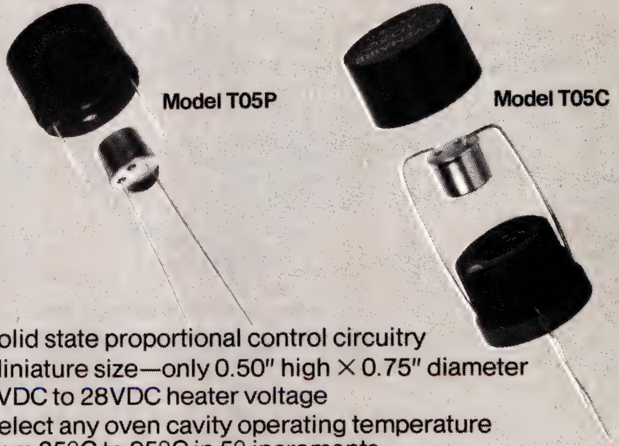

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A CROWD OF HOPEFULS WARMS UP FOR 32-BIT MICROPROCESSOR RACE

by Bernard Conrad Cole

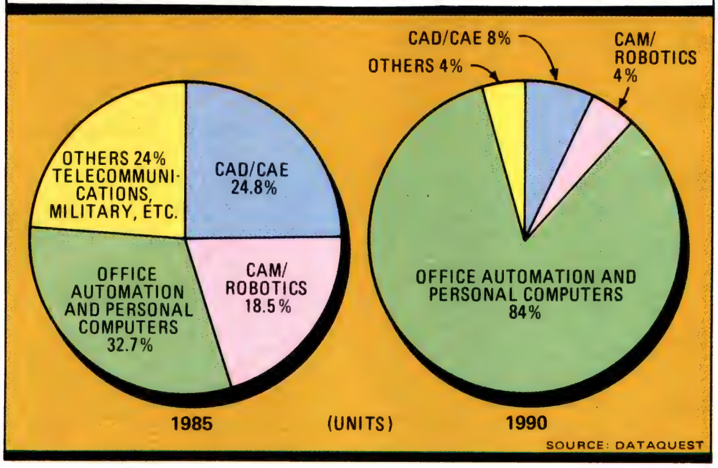
NUMEROUS DESIGNS ARE IN THE WORKS, BUT INDUSTRY CAUTION AND PROCESSING DELAYS HOLD BACK ALL BUT THREE

When semiconductor and computer-systems manufacturers talk about 32-bit microprocessors, they give the impression that they are involved in a life and death conflict—symbolically, of course—for domination of the marketplace. They see themselves as participating in a market war that could determine, for the rest of this century at least, the commercial pecking order in the electronics industry.

The list of potential applications and the projected total market size would seem to bear this out. Most estimates of the 32-bit market in the mid-to-late 1990s approach several billions of dollars in central-processing-unit sales alone, and the tens of billions when peripherals, software, and development systems are included.

Initially, the largest market segments will be in business applications and office automation, engineering work stations, and numerical control—functions now performed by high-end 16-bit microprocessors (see pie chart, below). A second wave of applications consists of those now requiring the power of large mainframes and superminicomputers, including expert systems, robotics, video graphics, transaction processing, signal processing, multiprocessing, and speech recognition. In the third wave there will emerge a 32-bit home and personal computer market built around sophisticated but easy-to-use expert-system-, natural-language-, and graphics-oriented software, which is expected to appeal to the broad base of users who find learning computer skills too difficult or time-consuming.

OFFICE USE OF 32-BIT MICROPROCESSORS WILL BOOM BY 1990



SOURCE: DATAQUEST

Thus far, however, World War 32 is all talk and little or no action. Of the perhaps two dozen or so 32-bit processors, only three commercial versions are actually available on the open market. Although they have not made them available on the outside, many systems houses have developed 32-bit microprocessor versions of their larger systems and have been producing them for internal consumption for several years now. But for all that experience, they are approaching the open market with extreme caution.

According to Mel Thomsen, senior semiconductor industry analyst for Dataquest Inc. in San Jose, Calif., the market for 32-bit processors is insignificant at present.

"When this market develops depends in part on how well the various micro manufacturers implement their production strategies," says Thomsen. "So far, most have slipped in their introduction times for the more sophisticated parts in terms of processing. Though the first-generation suppliers of 32-bit processors such as National and Motorola are now supplying parts in the 6-to-10-MHz range, this is not enough. The markets they are aiming at are performance-driven, and they require CPUs with clock speeds in the 12-to-16-MHz range initially, and eventually 25 MHz. However, this kind of performance is difficult to achieve and everyone is having problems." As a result, Thomsen has revised his estimate of the size and growth downward, slipping the schedule for production starts by 9 to 12 months.

From early estimates of 100,000 to 150,000 microprocessors shipped in 1985, the actual figures will be about 10% to 15% less. Dollar value is hard to estimate, since a lot of pricing is artificially inflated. Based on unit pricing averaging $250 to $500 each, estimates are that 1985's total sales will be about $20 to $50 million. This is barely enough, Thomsen says, to pay for the research and development on the various devices.

"And while the units shipped will continue to increase, it will be much slower than most people expect," he says. "Moreover, once the number of competitive devices in production begins to increase, the unit price will drop drastically." Because of the longer development time required for 32-bit designs, volume will not increase significantly, at least not enough to offset the reduction in price.

Thomsen estimates that by 1989 or 1990, the number of 32-bit CPUs shipped will be roughly 1 million per year. This will translate into no more than $200 million in sales. Adding in sales of peripheral circuits, software, development systems, and so on, the total sales relating to 32-bit systems will be around $1 billion.

Some people in the industry put this figure higher, around $2 billion to $3 billion, basing their estimates on the 4:1 drag effect—that is, traditionally, for every $1 of CPU sales, microcomputer vendors have been able to generate an additional $4 for support circuitry. However, Thomsen believes that for the 32-bit market, this is no longer true.

"Because of their complexity and density, there will not be as many peripheral chips associated with the CPU," he says. "Moreover, aside from some specialized peripheral functions, most general peripheral functions will be handled by slave processors, both 8- and 16-bit."

The main combatants in the first stages of the 32-bit war are National Semiconductor Corp., because of its early commitment, and Motorola Inc., because of the existing base of 16-bit users it has built up. New contenders, scheduled to be in production late this year or early next year, include Intel, Zilog, and AT&T (see table, p. 52).

The National 32032 (Fig. 1) is an attempt to implement in silicon a full VAX-type pipelined minicomputer architecture. Featuring virtual-memory support and a highly regular (orthogonal) instruction set designed for high-level-language support, the 32032 works with external memory-management and floating-point processors. With uniform addressing of up to 16 megabytes of random-access memory, its instruction set has been designed for symmetrical access to all data types as well as all register locations and memory types. Advanced features include demand-paged virtual memory, position-independent read-only-memory code, and multiprocessing support.

Introduced in late 1983, the 32032 has established a clear lead with almost 1,500 design-ins. National has taken a conservative implementation approach, using its well-understood and mature 3.5-μm n-MOS process; for coming generations, it will migrate to a 2-μm CMOS process. The 32032 is currently available in 6- and 10-MHz versions. When the die is shrunk in n-MOS, the whole family will be upgraded to a 15-MHz clock rate. A 25-MHz clock rate is the goal for the CMOS versions.

Combined with the impressive number of design-ins and its second-source agreement, National has, in the view of many of its competitors, a good chance for success in the 32-bit world, but only if it "makes no stumbles and commits few mistakes," says Thomsen. Set for introduction later this year is the 32132, with on-chip bus-arbitration logic for tightly coupled dual-processor designs. Due in late 1986, the 32C432 is a CMOS CPU with on-chip memory management and cache.

Introduced in mid-1984 to protect its base of potential 16-bit 68000 upgrades from National, Motorola's 68020 is a full 32-bit version of the 68000 that runs existing object-code-compatible software (Fig. 2). Fabricated using the company's HCMOS process, it runs at 16.67 MHz and features an on-chip instruction cache, 4 gigabytes of virtual memory, dynamic bus sizing, and a barrel shifter to speed execution.

With four levels of pipelining, multiple instructions can be in various stages of execution concurrently. It features an asynchronous bus with 32 address and 32 data lines. A 25-MHz version will be available as samples in late 1986.

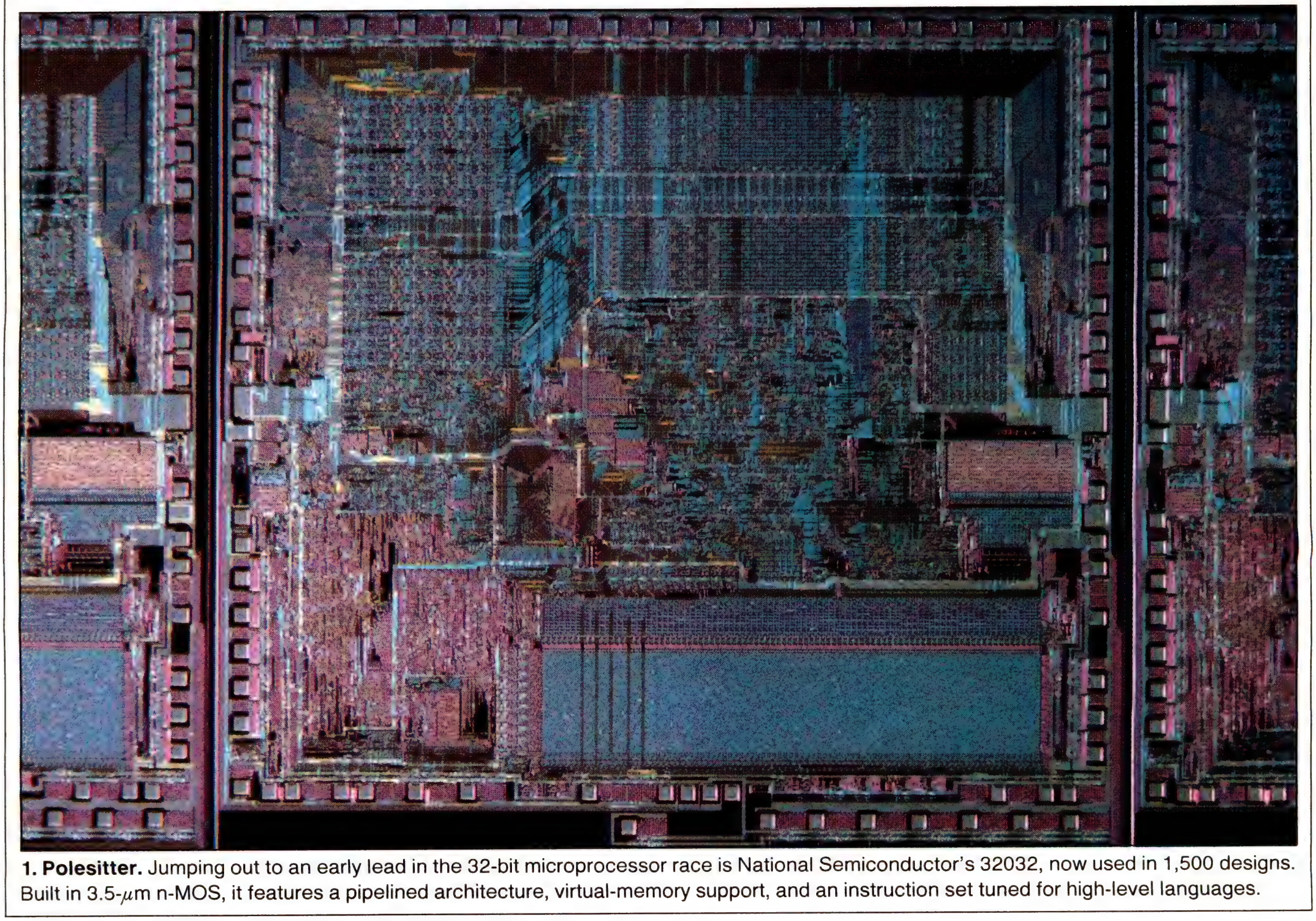
Claiming more than 500 design-ins, Motorola is in a solid second position, with the potential to gain further design-ins quickly as a result of upgrades from current 16-bit 68000 designs. Currently, France's Thomson-CSF is the only second source for the 68020.

Some new contenders

By mid-1986, three additional microprocessors will be added to the line of battle—Zilog's Z80,000, Intel's 80386, and AT&T's WE32100. Each offers a challenge to the current front-runners for different reasons: Intel Corp. because of its huge base of 8- and 16-bit designs to draw on as a source of 32-bit customers; AT&T Co. because of its sheer size and long experience in production with its 32-bit CPU, albeit for internal consumption; and Zilog Inc. for the advanced features incorporated into its design.

If successful in marketing their second-generation designs, says Thomsen of Dataquest, they could seriously affect the plans of National and Motorola, which have established a dominant position with the first wave of products. Zilog's part could damage Intel's self-image—and its image in the marketplace—as a technology leader. According to engineers who have attended several of the design sessions now being held by Intel, the Z80,000 is the microprocessor Intel would have developed if it did not have to worry about maintaining upward compatibility with its existing product line.

With its Z80,000 (Fig. 3), Zilog is attempting nothing less



1. Polesitter. Jumping out to an early lead in the 32-bit microprocessor race is National Semiconductor's 32032, now used in 1,500 designs. Built in 3.5-μm n-MOS, it features a pipelined architecture, virtual-memory support, and an instruction set tuned for high-level languages.

FEATURES AND PROCESS TECHNOLOGY DETERMINE PERFORMANCE LEVELS OF 32-BIT MICROPROCESSORS

Processor	National Semiconductor NS32032	Motorola MC68020	Zilog Z80,000	Intel 80386	AT&T WE32100
Process technology	n-MOS	n-well CMOS	n-MOS	n-well CMOS	Domino CMOS
Design rules (μm)	3.5	2.25	2	1.5	1.5
Clock rate (MHz)	4/6/10	16.67	10/18/25	12/16	10/14
Throughput (mips)	1 to 2	2 to 3	1 to 5	3.5 to 4	0.5 to 1.7
Power consumption (W)	1.5	2	2	1.5 to 2.5	0.7
Instruction cache (bytes)	0	256	256	0	0
Data cache (bytes)	0	0	256	0	256
Address width (bits)	24	32	32	32	32
Data/address lines	multiplexed	nonmultiplexed	multiplexed	multiplexed	nonmultiplexed
Addressing modes	9	20	9	24	9
Memory management	paged	paged/segmented	paged (on-chip)	paged/segmented (on-chip)	paged/segmented
Number of instructions	86	65	110	111	169
Instruction queue	8 bytes	2 words	6 stages	4 levels	4 stages
Burst memory transfer	no	no	yes	no	no
General-purpose registers	8	16	16	16	16
Dedicated registers	8	8	0	0	0
Availability	now	now	1986	1986	now

than a quantum leap over existing and proposed 32-bit designs, both in terms of architecture and process complexity. Unlike many other 32-bit makers who are moving toward CMOS, Zilog has developed a special 2-μm n-MOS process featuring intrinsic transistors, high-value polysilicon transistors, and multiple levels of interconnection which, says Robert Andrews, director of marketing support for 32-bit microprocessors at Zilog, is important in achieving a clock speed of 25 MHz. "This process yields deliverable products with smaller dice and higher speeds than most CMOS implementations, and at a lower cost to the user," he says. "Equally important, it yields parts with power consumption roughly equivalent to the CMOS design parts from competitive vendors."

The Z80,000 has three attributes not found in the products from Motorola and National. First is a cache memory for both data and instructions, unlike the 68020, which has an instruction cache only, or the 80386 and 32032, which do not have either. On-chip cache minimizes memory accesses and thus reduces traffic on the bus. Caching both data and instructions generally improves performance by 20%, which is, according to Andrews, key in military and scientific applications.

A second key factor is the use of a six-level pipelining architecture. The third factor is on-chip memory management, providing 4 gigabytes of virtual memory space. The CPU is able to generate physical addresses, eliminating the delay inherent in external memory-mapping approaches.

With the Z80,000's hardware-interface control register and six on-chip programmable-wait-state generators, it is possible to specify selected characteristics of the hardware surrounding the CPU, including bus speed, data-path widths, and the number of wait states. External bus speeds can be set to run at the same speed as the CPU or at half speed, while the CPU runs at 25 MHz. "On the basis of technological innovation alone, Zilog has all the elements to make it a front-runner in the 32-bit market," says Howard Sachs, general manager of advanced processors at Fairchild Camera & Instrument Corp. "However, that may not be enough."

Scheduled for introduction during the latter part of this year with sample quantities during the first quarter of 1986, Intel's 32-bit 80386 (Fig. 4) is basically an extension of its 16-bit 80286 architecture with demand-paged virtual memory, an address range of 32 megabytes, and on-chip memory management of as much as 4 gigabytes—as well as extensive use of pipelining by means of an on-chip instruction queue. Unlike the present 68020 and Z80,000 and the future 32C432, the 80386 will not include true on-chip cache. Its main differences from the 286 are the use of HCMOS-III rather than HMOS technology, a 32- versus a 16-bit data bus, and a 32- rather than a 16-bit internal architecture. Three times faster than its 16-bit predecessor, the 386 will have a 16-MHz clock rate and run in the range of 3.5 to 4 mips.

To protect its customer base, Intel strongly emphasizes the higher system performance capabilities of its 286 compared to the 32032 or 68020. For example, says Bob Patterson, manager of Intel's 32-bit program, the 16-bit 286 can run at 1.4 to 1.5 mips versus just 1 mips for the 32032, with 6-MHz clock rates. And in a Unix environment, he says, a 10-MHz 80286 runs at 2.2 mips, roughly equivalent to a 16.67-MHz 68020. With a 12.5-MHz clock, the 286 can run at 2.7 mips.

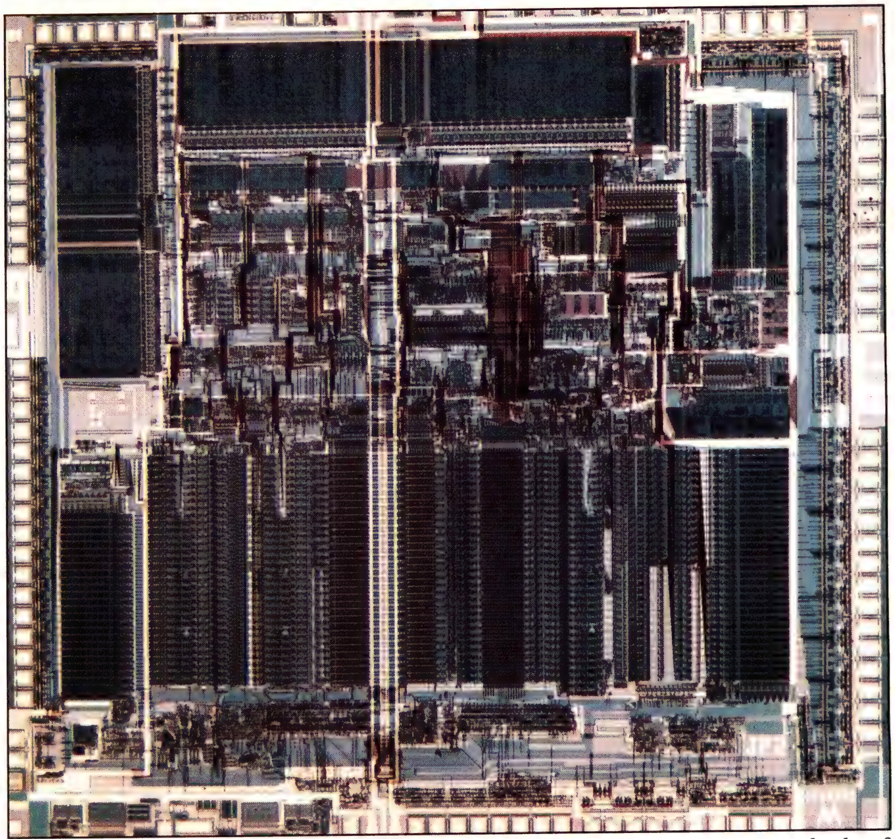
With its long production experience in fabricating the WE32100 and its various predecessors back to the Bellmac 32, AT&T's entry into the merchant market earlier this year establishes it as a potential front-runner in the 32-bit market. Fabricated using a 1.5-μm CMOS process, the merchant version of the WE32100 will be available for 10- and 14-MHz clocks. Though it is currently not being second-sourced, possible candidates for doing so include Mostek and GE/Intersil.

Impact of the captives

In addition to AT&T, at least three large systems companies have developed in-house 32-bit CPUs that can be considered significant: Data General Corp., Digital Equipment Corp., and Hewlett-Packard Co.

The microEagle is a five-chip VLSI implementation of Data General's 32-bit Eclipse architecture. Fabricated using a proprietary titanium disilicide n-MOS process with 2-μm design rules, the design runs about half as fast as the company's MV/8000 superminicomputer and supports 4 gigabytes of virtual memory. The CPU is a true 32-bit part with three-level pipelining; it contains an arithmetic-logic unit, 4 accumulators, 8 general-purpose registers, and 12 special-purpose registers, all 32 bits wide. An on-chip address-translation unit provides memory management in 2-K-byte pages, supporting a physical address space of 128 megabytes. The Eclipse instruction set is implemented on a separate microsequencer chip.

DEC has developed three separate 32-bit microprocessor implementations of its VAX superminicomputer architecture, all fabricated with a proprietary high-speed n-MOS process. They differ in chip count, amount of custom circuitry, and performance. The first implementation is the microVAX-1, a three-chip set consisting of the 32-bit CPU with off-chip microcode and a custom data-path chip. The data-path chip requires



2. Compatible upgrade. Motorola's 68020 is a full 32-bit version of the popular 68000 microprocessor that runs object code developed for its 16-bit predecessor and addresses up to 4 gigabytes. Built in a 2.25-μm n-well CMOS process, it uses a 16.67-MHz clock.

implementing the microcode with standard medium- and large-scale integration devices. A configuration implementing the entire instruction set on a single 50-chip board exceeds the performance of a VAX-11/730. The second implementation is the VLSI VAX, whose nine-chip set implements the full VAX instruction set with most of the CPU functions including memory management and cache control. Performance is roughly comparable to that of a VAX-11/780 CPU. The third is the Microvax-32, a single-chip implementation of a subset of the VAX instruction set, including memory management. When operated at a 20-MHz clock rate, it is about 20% slower than the VLSI VAX.

Probably one of the most advanced 32-bit processors yet manufactured, the Focus CPU from Hewlett-Packard is a 1-μm n-MOS device used only internally, first in the firm's 9000 minicomputer. With a full 32-bit architecture, it features demand-paged virtual memory, an address range of 500 megabytes, an 18-MHz clock, a 38-bit instruction word, and 230 instructions. Brought into production internally in late 1980, the Focus chip may already be out of date. Its successor is reported to be a 32-bit processor of the reduced-instruction-set-computer (RISC) type, code-named Spectrum.

"Many of the large system houses have developed their own in-house 32-bit CPUs out of self-protection," says Thomsen. "Initially, it was a matter of protecting their software base and their existing base of users by offering microcomputer-based versions of their mini and mainframe products. But the strategy is not without risks. Even if they start out just serving their internal needs, their micro-based products will be in competition with those based on CPUs from merchant vendors." This means increasing investment in research and development far beyond their internal requirements to remain competitive in performance. But cost is also a factor, and in order to also remain price-competitive, systems houses are being forced to "go public." So far, AT&T is the only one to break ranks, but pressures are increasing, says Thomsen, that will force the others into the merchant market.

According to Sarv Thakur, microprocessor product marketing manager at Hitachi America Ltd. in San Jose, the captive CPUs will play less of role as time goes on. "There are two reasons for this," he says. "First of all, the object-code compatibility and hardware dependence will be replaced by high-level-language and source-code compatibility as the major factors in software-base protection. Secondly, the gap between the technology available from commercial semiconductor vendors and the captive in-house facilities is likely to widen due to competitive market forces." In other words, while the merchant suppliers initially will be forced to play according the system houses' software-support rules of combat, as time goes on it will become the performance-driven process-based game the merchant vendors are expert at playing.

"The captive CPU vendors can successfully go public only if they make a major departure from low-level compatibility with their existing systems, and if they can convince OEM's that they would commit to support them at the same level as their own in-house users," says Thakur. However, both of these factors are in conflict with the obvious strategies of the captive CPU houses and the likelihood of such developments, says Thakur, is relatively small.

As a result, Thakur says, while the closed markets now represent a dominant share of the total, by the early 1990s this ratio will change sharply, with more of the closed market becoming accessible to the merchant suppliers. By 1995, he thinks, the open markets will represent 80% of the total.

Going their own way

At least three companies with 32-bit designs have decided not to compete directly with general-purpose designs: Advanced Micro Devices, NCR, and Inmos. Instead, each has targeted niche markets for which it has developed specialized designs: AMD for superminicomputer and graphics processing; NCR for mainframe emulation, in particular IBM designs; and Inmos, for multiprocessing applications.

Developed orginally for use internally, the NCR/32 is an n-MOS bit-slice chip set 32 bits wide aimed at minimum-chip-count mainframe and minicomputer emulation. CMOS versions are now under consideration.

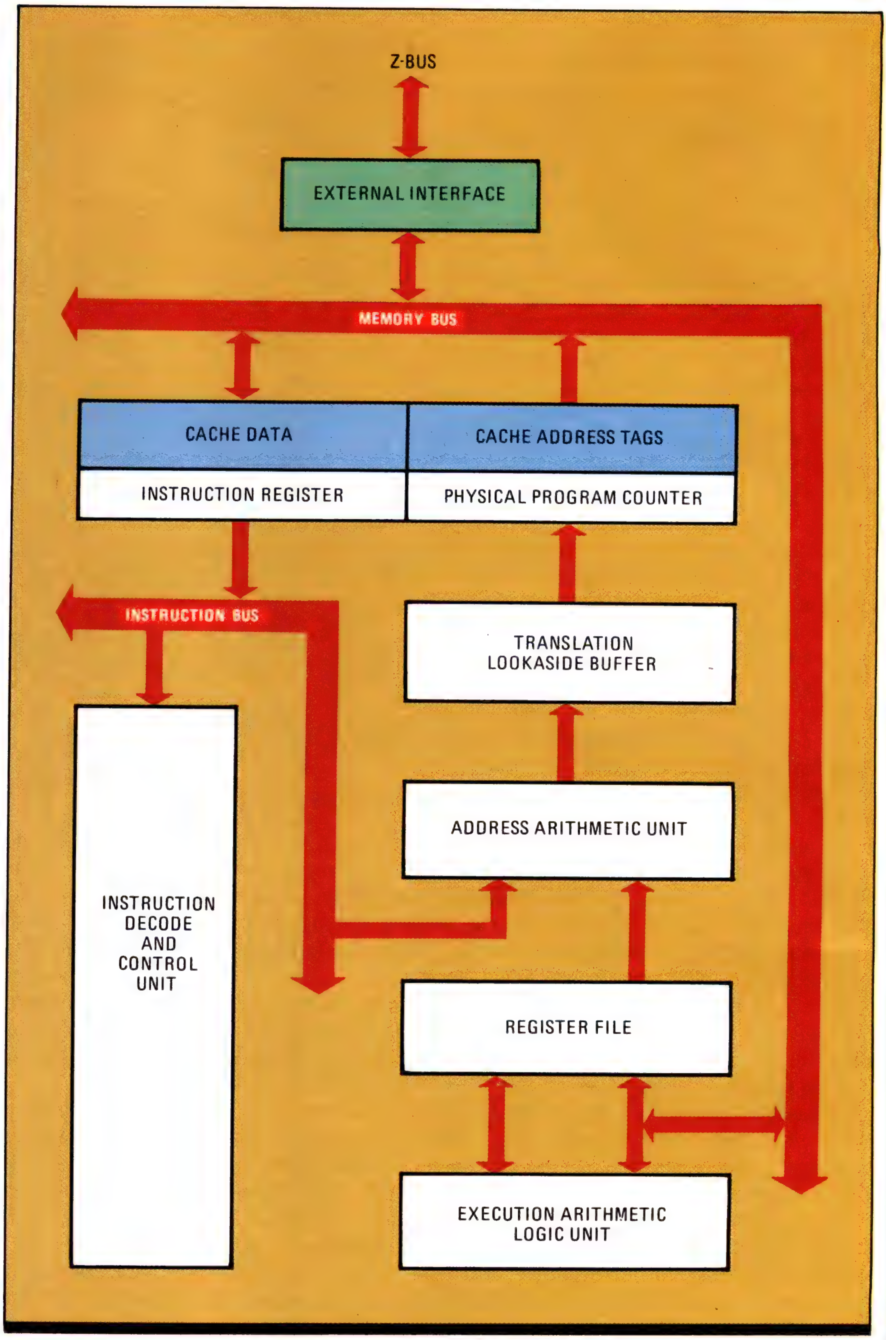
The set consists of four VLSI circuits: a 32-bit CPU, an address-translation chip, a floating-point chip, and a system-interface controller. In addition, a 128-K-byte external ROM device, called the instruction storage unit, carries the external microcode needed to tailor the chip set to the user's needs.

The CPU executes 179 primitive instructions in a three-stage instruction pipeline. At 13.3 MHz, the NCR/32 runs IBM MVS software at about the same speed as an IBM 4331. Emulating the DEC VMS environment, it is about five times slower than a VAX-11/780. Using its own native code, the NCR/32 is about three times faster than a VAX.

Aiming at even higher performance, the AMD 29300/29400 32-bit bipolar function-slice family is aiming at minimum-chip-set configurations with 3 to 10 times the performance of a VAX-11/780. It follows the building-block philosophy of the 2900, except that all chips have a fixed 32-bit data-path width.

Available in late 1985, the initial offering is the 29300 with

3. Ambitious. Zilog hopes to leapfrog the competition with its technically advanced Z80,000, which features an on-chip cache and memory management and six-level pipelining. The firm is developing a special n-MOS process aiming at 25-MHz operation.



internal emitter-coupled logic and TTL interface circuitry, capable of 70-to-80-ns cycle times. The 29400 is an even faster version with ECL input/output and capable of 40-to-55-ns cycle times. AMD is also considering high-speed CMOS versions.

Fabricated using a 2-μm CMOS process, the Inmos T424 transputer is a 32-bit RISC CPU with 4-K of on-chip cache, designed for use in multiprocessor systems and data-flow implementations using multiple processors. Clocked by a 5-MHz signal, the T424 executes just one instruction format, calculated at almost 80% of the typical executed instructions in an average system. Each CPU has multiple high-speed communications channels, allowing it to be connected to others with a minimum of interfacing logic. Each transputer has at least four full-duplex links on chip, making it possible to build multitransputer systems of any size.

As if the 32-bit battlefield were not already crowded enough, numerous other implementations are in development, many of them employing RISC architectures. Now under development and approaching sampling stages is a 32-bit RISC from Fairchild, code-named Clipper. Said to run at a blazing 40 MHz, this CMOS device's data bus, operands, and registers are all 32 bits wide.

Other commercial 32-bit RISC CPUs include IBM's ROMP and 801 IMP; a 32-bit gallium arsenide CPU from McDonnell Douglas Corp.; and a 32-bit RISC chip under development by TRW Electronic Systems under the auspices of the Department of Defense's Very High-Speed Integrated Circuits program.

There is also a variety of Japanese 32-bit CPUs under development by Hitachi, NEC, Fujitsu, Matsushita, Toshiba, and Mitsubishi. Closest to sampling stages are Hitachi Ltd.'s Micro32 and NEC Corp.'s V series.

Hitachi's 32-bit CMOS CPU contains full 32-bit address and data buses, a 32-bit arithmetic logic unit, and 200-K of on-chip ROM. Upwardly compatible with Motorola's 68020, it is supposed to be able to operate at 5 mips. The company hopes to offer samples by late 1986 and be in production by 1987.

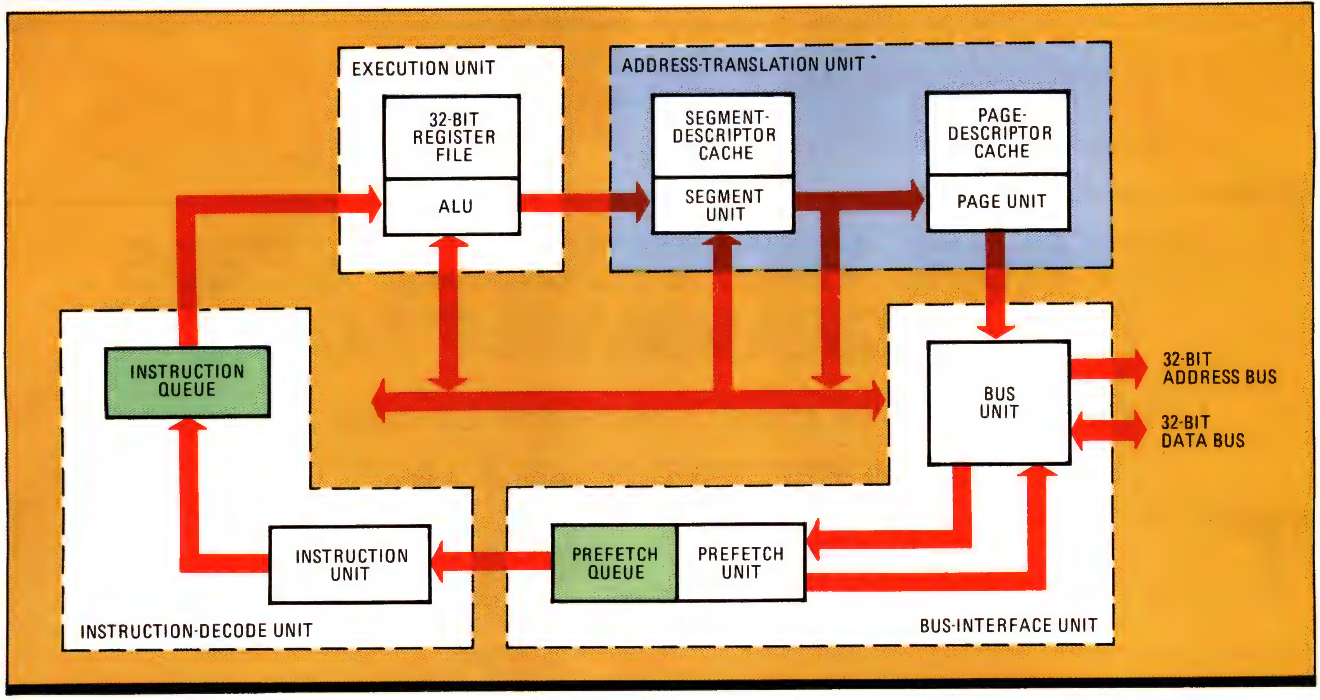
NEC is currently developing its V series, designed to be upwardly compatible with Intel's 286/386 chips. It expects to be out with the V-70 32-bit CPU by the first half of 1987.

Thomsen predicts that the market for 32-bit chips will grow larger than that for 8- and 16-bit microprocessors combined. The best gauge of how the 32-bit market will evolve, he says, is to look at the evolution of previous generations of microprocessors, particularly the 8- and second-generation 16-bit units. Historically, he says, the product-acceptance curve for second-generation 16-bit chips was identical to that for 8-bit units. For example, the shipments of such 16-bit processors as the 8086 and the Z8000, introduced in 1978, did not begin to grow in the marketplace and show themselves in volume in end systems until 1983. And even by the end of 1984, 16-bit processors represented only 12% of all microprocessors sold.

"Extrapolating from that to the 32-bit market, we can expect to see a similar slow, evolutionary growth, with the market beginning to take off about four to five years after their introduction, about 1988-89," says Thomsen. "It will only begin to be dominating in terms of market share by the mid-1990s." Until then, it will grow relatively slowly, as design-ins accumulate and system designers have a chance to assess, compare, and completely understand the architectural trade-offs among the alternative designs.

"While the various manufacturers of these 32-bit machines are optimistic about promise, as well they should be, this promise will be realized much later than most of them think," says Sachs of Fairchild. "Remember, in many respects these devices are mainframes on a chip, extremely complex devices, with volumes of documentation and much in the way of development systems, software, and other aids to master."

The current market, then, can be characterized as being in a positioning phase. Product families are being introduced,



4. Hold the fort. The 80386 is a major factor in Intel's defense of its huge 8- and 16-bit customer base. To be built in the firm's HCMOS-III process and running at 16 MHz, it is said to have about three times the performance of the 16-bit 80286 and will have on-chip memory management.

alliances being made, key customers courted; companies are telling their stories and outlining the parts they have and will have as well as their product-introduction strategies.

"What is holding the market back right now is the sheer complexity of these devices and the number of different devices which have been introduced," says Thomsen. "Any designer contemplating the use of a 32-bit processor would be jumping the gun if he made a commitment this early. There are just too many alternatives and the best is yet to come, if some of the preliminary specifications are to be believed."

In the 8-bit world, in which as many as 10 major architectural variations were introduced, five products now account for 85% of the market, Thomsen points out. In the 16-bit market, four out of six major CPU types initially introduced now also account for 85% of the market.

"When you include the captives, the Japanese, and various CPUs just now emerging from various universities and private research labs, there are about fifty 32-bit devices introduced or under development, five times the number of 8-bit devices introduced and eight times that in the 16-bit world," he says. "This means that at some point there is going to be an awful lot of blood drawn."

In the long run, a similar evolution will occur, with perhaps five parts occupying 80% of the market, and the rest crowded into the remaining fifth. However, given the ultimate size of the 32-bit market, that 20% will be enough for quite a few to survive and thrive, says Thomsen.

Vendors that are strong at 8 and 16 bits will have an opportunity to be among the major players. But just as new vendors made it into the main arena with the arrival of 16-bit processors, so will they at 32 bits. National may be present thanks to its tremendous and early commitment; IBM and Intel have a leg up because of their personal computer dominance; and Zilog may shine because of the Z80,000's technical advantages. AT&T is also a major factor, says Sachs, because of its sheer size, the fact that the operating system of choice at 32 bits will be its own Unix, and because it has been in production with a 32-bit processor longer than anyone else.

Predicting who will be the leader of the pack depends on which application, market segment, and stage of the evolving 32-bit marketplace is considered, says Thomsen. There are four large markets foreseeable for microprocessors.

One market is the existing base of 8-bit users, for whom 8 bits is enough and may even be a bit of overkill. The need for additional performance in this area can be met merely by faster 8-bit engines. Many, but not all, will migrate upward, not just for the performance, but to take advantage of the more sophisticated applications software available.

A second set of users consists of those who started at the 16-bit level because that was the only way to get the performance they needed. Their applications include work stations for computer-aided design and -manufacturing, office automation, and high-end personal computers. Primary CPUs include the 68000, 68010, the 16016 and 16032, and a few Z8000s and 80286s. This category will constitute the bulk of the 32-bit market in the initial stages over the next few years, going mostly to upgrades such as the 68020 and 80386.

The third group is the traditional users of minicomputers. With their strong backgrounds in software, these users understand many of the concepts and techniques, such as pipelining, memory protection, virtual memory, and cache, incorporated into the 32-bit processors. Here, advanced versions of existing products as well as new designs such as the Z80,000, Fairchild's CPU, and some of the novel Japanese architectures will be starting out on equal footing.

A huge untapped market

A fourth category includes totally new designs not possible with present systems and cutting across all application boundaries. In personal and home computers, such systems will combine the power of 32-bit processing with the new software for expert systems, image processing, signal and speech synthesis, communications processing, large memory capacities, and gigabytes of disk storage—all decreasing in cost.

"When this happens, we will see an explosion of computing into the 90% of the mass market not now accessible," says Thomsen. This market, which is expected to mature by the end of the century, is totally up for grabs.

"Who will dominate in this fourth category is totally unpredictable. It depends in part on who survives the earlier cycles, and in part on who makes the necessary investment in software development to make those applications happen." ☐

SEMICONDUCTORS

EEPROM TECHNOLOGY SEEDS REPROGRAMMABLE LOGIC

LATTICE'S GAL16V8 USES A HIGH-SPEED CMOS PROCESS TO REALIZE A REPROGRAMMABLE LOGIC ARRAY

The technology used in electrically erasable programmable read-only memories, which are growing in popularity wherever nonvolatility and erasability are needed, is now hitting pay dirt in the logic arena as well. Designers at Lattice Semiconductor Corp., Portland, Ore., have paired EEPROM technology with a high-speed CMOS process to build programmable logic devices. The programmable chip relies on EEPROM cells for an electrically alterable architecture so it can directly replace any of 21 device architectures in the 20-pin bipolar PAL family manufactured by Monolithic Memories Inc.

The GAL16V8 (for generic array logic) is said to run at bipolar speeds—25-ns propagation delay—with an output drive of 24 mA, using EEPROM cells in place of normal fuses (see photo below). This results in an electrically reprogrammable, reusable device that can be programmed on standard logic-array programmers using supporting software such as ABEL, which is provided by Data I/O Corp. in Redmond, Wash., and CUPL, provided by Assisted Technology Inc. in San Jose, Calif.

GAL16V8s can be used repeatedly during system prototyping. The same GAL16V8 used in one type of logic circuit can be reprogrammed for use in another circuit. Because of its output logic architecture, each individual output can be tailored as registered, combinational, active high, active low, input only, or bidirectional.

Dean Surh, manager of Lattice's Programmable Logic Product Engineering Division, says that the EEPROM cell in the GAL16V8 exhibits excellent data retention and endurance characteristics. He also says that the cell's design has been proven at Lattice in several large memory chips, including a 45-ns 64-K EEPROM.

"Unlike bipolar fusible-link devices, the 16V8 cells require no openings in the passivation for fuse debris to escape, nor are they subject to the 'grow-back' phenomenon of fuses," he notes. "This results in improved reliability." In addition, the cell writes quickly: an erase-and-program cycle of a 16V8 cell takes 20 ms.

Programmable logic devices place a stringent requirement on technology: circuits need to be extremely fast, current drive extremely high, and programming elements extremely reliable. Fusible-link bipolar technology once stood alone in meeting those requirements.

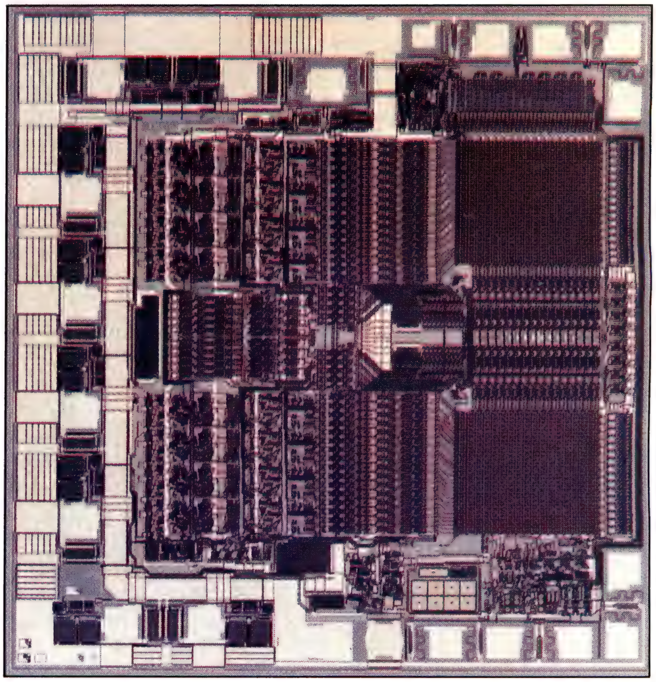
But Rahul Sud, chief executive officer of Lattice, says that is no longer the case. "Today, high-speed electrically erasable CMOS is the technology of choice for programmable logic," he told *ElectronicsWeek*.

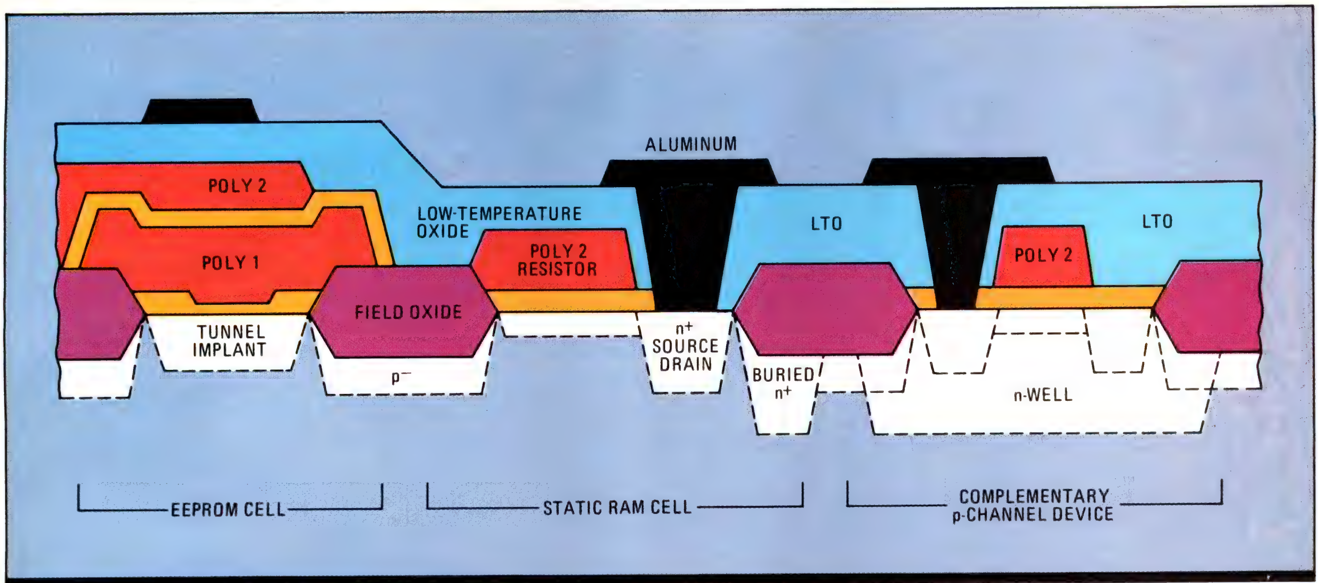
Sud calls his process UltraMOS. He points out the advantages of EEPROM cells for the nonvolatile programming elements over fuse links: a nondestructive nature for reusability and, thus, testability; the low programming current required, making possible the on-chip programming-signal generation key to next-generation in-circuit-alterable components; and reduced contamination through complete passivation of the chip, promoting greater reliability.

Some CMOS-chip makers have chosen EPROM cells, which require ultraviolet-light exposure for erasing, as the programming element in their PLAs. Although it has certain advantages over bipolar fuses, EPROM technology falls short of EEPROM when it is applied to programmable logic (see table); it is also not applicable to future architectures that will require in-circuit reprogrammability.

Sud explains that from the manufacturer's standpoint, EEPROM technology holds significant cost advantages over EPROM technology in building programmable logic devices. Although he admits it is a more complex process, EEPROM technology "affords significant savings in the cost of testing, since cells can be programmed, erased, and reprogrammed in milliseconds, whereas EPROM cells require 20-min ultraviolet-light exposures for erasure." Moreover, he continues, "though EEPROM is a less dense technology than EPROM, memory-array area has little impact on die size in a PLA, where some 90% of the chip comprises random logic."

The implications of a reconfigurable logic device in the engineering lab environment are significant. In the past, every design revision, checkout, or upgrade required pulling a





Modular. UltraMOS has been designed modularly, so steps in the flow may be eliminated if elements such as the load resistors are not needed. The process uses the first level for floating-gate EEPROM cells and the second level for load resistors and enhancement and depletion gates.

new PLA from an inventory stock of some 21 different architectures, with three speed/power options for each architecture. The PLA was patterned with the new logic, then tested for the first time for full functionality.

The old PLA was discarded because its fuse-link cells could not be reused. The GAL16V8 eliminates the need for the expensive inventory that is required for full-line support, thanks to its single-device replacement approach, 100% fuse-map compatibility, and performance that is superior to the current bipolar data devices.

The 16V8 can be repatterned and reused in less than a second, as opposed to the 15 to 20 minutes that are usually required. The EEPROM cells can be patterned for worst-case data-sheet performance during testing to fully guarantee, through actual test, performance over all data-sheet conditions without having to resort to correlated or simulated paths in the device.

"Because the GAL 16V8 is compatible with the 21 most popular programmable logic arrays, it can be substituted into existing system designs in a completely transparent fashion," according to Surh. "The replacement is 100%, in terms of performance specifications, logic functionality, and fuse-map compatibility."

These same inventory and universal configurability benefits are available to the production and field-service staff. They, too, can employ the GAL16V8 as a single, reusable replacement for dozens of PLAs. Field modifications, service, upgrades, and functional changes can be made with only one device type.

The GAL16V8's output logic macrocell (OLMC) allows it to be configured in a number of ways that are not possible with ordinary PLAs, according to Lattice engineers. For example, because a synchronous (registered) output can be placed on any or all output pins, the user can create a variety of devices—a 16R1 or a 16R5, for example. These architectures are not possible with the ordinary PLAs that are currently available, say Lattice designers.

Lattice's UltraMOS is a basic CMOS EEPROM process that adds modules for high-resistivity polysilicon loads and for a buried n+ interconnect layer. A double-polysilicon process, UltraMOS (see figure) uses the first level for floating-gate EEPROM cells and the second level for all regular enhancement and depletion gates, as well as for high-value load resistors.

UltraMOS has been designed in a modular fashion. Therefore, steps in its flow may be eliminated with no impact to temperature cycles if certain elements, such as the polysilicon load resistors, are not desired.

Minimum features of the process extend down to 1.25 μm, with the smallest gate length currently limited to 1.5 μm. As PLAs move to 24-, 40-, and 84-pin densities, the package and device reliability, power dissipation, and exceedingly long programming time for the larger arrays all serve to dissuade further pursuit of this technology.

User-programmable logic continues to enjoy steady growth: sales this year are expected to approach $400 million. According to Sud, the reason for this growth is mainly time to market—computer-aided-design tools cannot compete with off-the-shelf silicon for turnaround time. The market for programmable logic is expected to hit more than $1.5 billion by the end of the decade, with the lion's share going to Monolithic Memories. The GAL16V8 targets the millions of 20-pin PAL sockets. □

COMPARING LATTICE'S GAL AND MONOLITHIC MEMORIES' PAL

	GAL 16V8	PAL devices
Speed	25/35 ns	25/35 ns
Maximum active current	90 mA	180/90 mA
90 mA at 25-ns specification	Yes	No
Technology	CMOS, E^2 cells	Bipolar, fuse link
Reprogrammable	Yes	No
Fully tested fuse array	Yes	No
Guaranteed reliability	100%	99%
Devices needed to supply full line	1	More than 20
User signature	64 bits	None
Configurable architecture	Yes	No
"Odd" architectures available	Yes	No
Configurable outputs	Yes	No
Security	Visual and electronic	Electronic
Programming time	3 s	12 s

SOURCE: LATTICE

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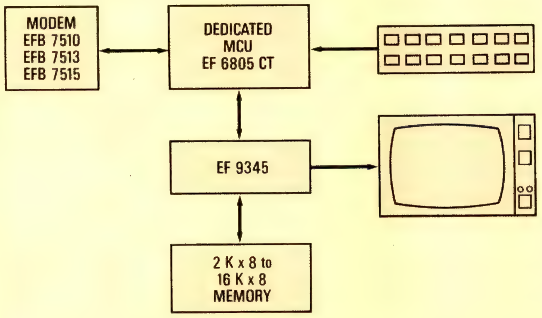

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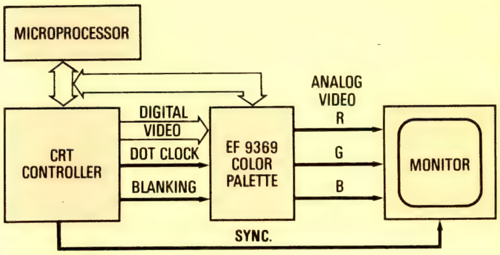

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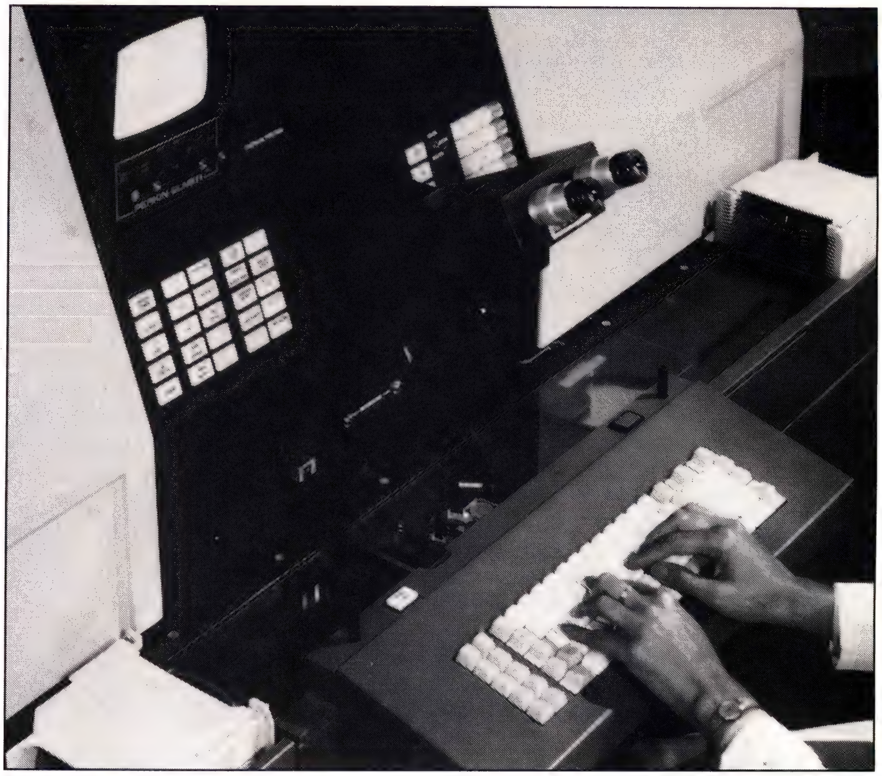
OPTICAL LITHOGRAPHY GEAR KEEPS PACE WITH NEW DEMANDS

A roundup of new equipment that meets the call for submicron features

Semiconductor manufacturers can remodel their houses—or at least their yellow rooms—with the latest lithography equipment unveiled at last week's Semicon West show in San Mateo, Calif. All of the products have made advances in three critical areas of concern to IC designers: resolution, wafer-size capability, and throughput.

Yet another concern addressed by the new systems is defect density. Vendors increasingly are automating facets of the wafer-production process, thereby decreasing particulate contamination. The ultimate goal is a people-less integrated wafer-fabrication line. In addition, new inspection systems have emerged that keep pace with IC designers' demands for precision and speed.

According to figures prepared by Rick Ruddell, an industry analyst and president of Ruddell & Associates Inc., Trinity Center, Calif., the market just for wafer steppers in 1985 will be $600 million, growing to $860 million in 1988.


Particle-free. Using an automated wafer-handling system, the Nanoline 5 line-width inspection system from Nanometrics keeps wafer contamination at a minimum.

Said to be fully automatic, the PAS-2500 system from ASM Lithography Inc. offers 0.9-μm working resolution with an overlay accuracy of 0.1 μm. The wafer-stepper system is the fruit of a joint venture between ASM's parent, ASM International, and N.V. Philips, both of the Netherlands. The system was developed by Philips and is being marketed by ASM Lithography.

The PAS-2500 takes advantage of a through-the-lens self-compensating laser-alignment technology to achieve its overlay accuracies from any one layer to another. The technique also eliminates drift and the need to recalibrate the system at regular intervals, says James W. Alexander, ASM's vice president. "Using the industry rule of thumb, overlay accuracy must be one fifth of circuit-line width to achieve optimum yields. The PAS-2500 comfortably measures up to the rule for processing 1-μm geometries," he says.

The wafer stepper features an exposure field of 20 mm in diameter using a Zeiss 46 lens as standard. A Zeiss 52 lens is optional, and other lenses can be used without modification.

Typical throughput for 6-in. wafers is 75 per h. An electromagnetically driven stage covers a 1-cm step in 200 ms, about 25% faster than competitive systems, Alexander says. The PAS-2500 will be priced starting at $800,000 when it becomes available early next year.

High throughput at submicron resolution levels is characteristic of two systems being offered from Perkin-Elmer Corp. Both the SRA-9000 step-and-repeat alignment system and the 600 HT Micralign projection mask aligner handle 6-in. wafers.

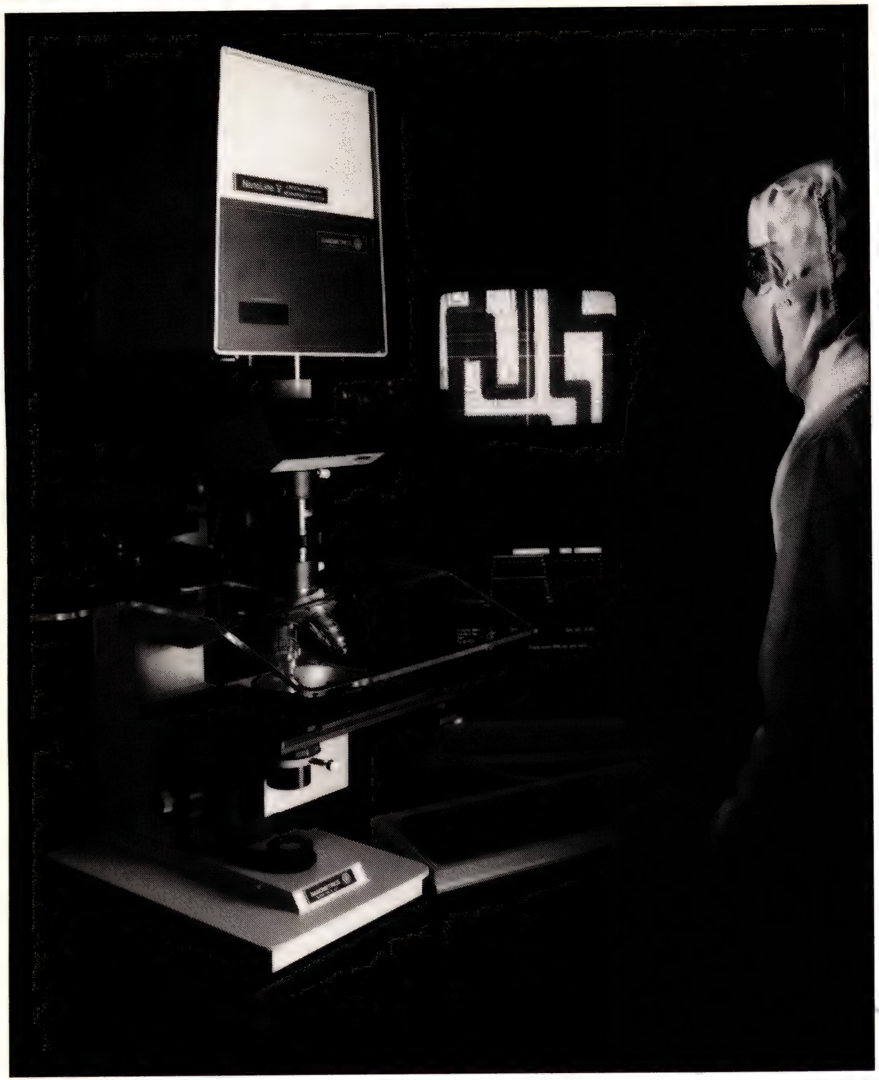
The SRA-9000, a 5× system, has a 5-in.-wafer production throughput—including alignment and leveling at each exposure field—of up to 70 units/h. The system employs as a backup a laser-stage/global-alignment system, which when used in conjunction with the standard field-by-field alignment system, maximizes process latitude. It is automatically engaged if the primary field-by-field alignment signals fall below the required levels. Field-by-field alignment accuracy is ±0.15 μm; laser-stage/global-alignment accuracy is ±0.35 μm, or 98% of the data, Perkin-Elmer claims.

Guaranteeing a low particulate specification, the 600 HT has a machine-to-machine overlay accuracy of ±0.35 μm, 98% of the data population. It provides throughputs of 100 6-in. wafers/h or 120 4- or 5-in. wafers/h.

The 600 HT's backside pick-and-place autoload wafer-handling system substantially improves die yields by minimizing defects resulting from particulate generation. The system completely eliminates contact with the edge and front surface of the wafer and boasts a certified particulate specification as low as 10 particles greater than 1 μm added per pass.

A family of new lenses lets GCA Corp.'s recently introduced model 8000 DSW wafer-stepper system achieve line resolutions of 1 μm or smaller. Alignment accuracy of ±0.02 μm is obtained with a new, digitized direct-reticle-reference alignment system. Users have the option of high-speed, fully global alignment with an accuracy of better than ±0.03 μm with the stepper's integrated alignment system.

Reduced particulate generation results from GCA's backside wafer handler and minimal-contact wafer-transport system. Throughput is 44 units/h for 5-in. wafers and 30 units/h



Fast. Handling wafers up to 6 in. in diameter at 100 units per hour, the Micralign 600 HT projection mask aligner from Perkin-Elmer also processes 5-in. wafers at 120 units/h.

for 6-in. wafers. Systems, which will be available in the second half of the year, are priced starting at $900,000.

In the area of wafer-measurement and -inspection equipment, Nanometrics and Nikon showed new gear. Using fluorescent light, Nanometrics' Nanoline 5F line-width measurement system makes precise photoresist measurements down to 0.5 μm. Photoresists fluoresce when they are exposed to blue or ultraviolet light, emitting light in the green or orange regions of the spectrum. Other materials on a silicon wafer do not fluoresce, however, and therefore appear black when the exciting light is filtered out.

The resulting high contrast and sharp edges between the fluorescing photoresist and the black background allow high-precision measurements of submicron features to be made; such precise measurements are not possible with conventional bright-field systems.

"We thought we had reached the lower limits of optical line-width measurement, but the Nanoline 5F has made it technically possible to challenge the measure-only scanning electron microscope market at greatly reduced cost to the semiconductor manufacturer," says Dave Zaring, Nanometrics' marketing manager.

A second system equipped with an automatic random-access cassette wafer-loading and unloading capability, the Nanoline 5 optical line-width measurement system answers the growing need for wafer-fabrication automation in order to decrease contamination and increase yield. The Nanoline 5 allows 4-, 5-, and 6-in. wafers to be loaded randomly from a cassette. To further decrease operator proximity to the wafers, every system is equipped with a motorized nosepiece, which eliminates the need for manual rotation of the turret when changing magnification. A computer automatically focuses the system by moving the motor-driven turret containing the lenses up and down in small steps.

Nikon uses its vast experience in optics and employs a hands-off wafer-transport system in its Optistation IC-wafer-inspection system that increases throughput and eliminates wafer damage and contamination. In operation, the Optisystem uses a noncontact photosensor to accurately prealign each wafer for inspection. A vacuum-chuck arm puts the wafer on a motor-driven stage, which moves the wafer through the inspection sequence. After inspection, a second arm unloads the wafer onto a urethane belt.

Long threatened by electron-beam lithography and X-ray lithography, optical lithography nonetheless continues to withstand the challenge. With gains in alignment technology, today's new systems easily handle 1-μm lines and are being pushed to the submicron regions. Many industry experts think that optical lithography will begin to run out of steam when 0.7- to 0.5-μm geometries are demanded. Hedging its bet, Perkin-Elmer is readying a direct-write electron-beam system developed under the Department of Defense's Very High Speed Integrated Circuit program.

Called Aeble-150, it will reliably produce IC devices with 0.5-μm features in production environments with a throughput of up to 30 wafers/h. The system, which Perkin-Elmer claims to be the first commercially available, has an overlay accuracy of 0.1 μm and critical dimension control of 0.05 μm. It features automated wafer handling and can work on wafers 6 in. in diameter.

But according to Ruddell, direct-write electron-beam lithography will be only a niche market. For the longer term, Ruddell says, "Everyone is serious about X-ray lithography," and he predicts that systems will be in use by 1987. "Ion-beam systems for repairing masks are popping up and are a critical piece in the X-ray puzzle." For the next few years, however, reduction steppers will soon be the workhorse, replacing step-and-repeat systems, Ruddell says. *–Steve Zollo*

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ASM Lithography Inc., 2315 W. Fairmont Dr., Tempe, Ariz.
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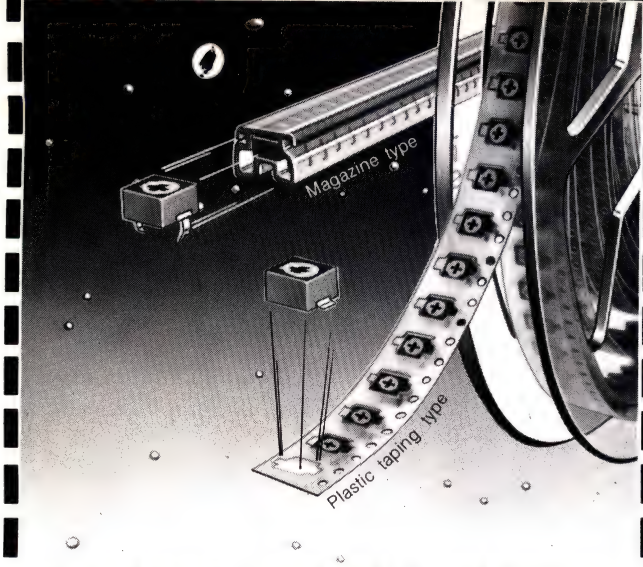

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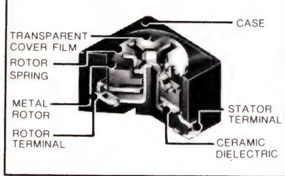

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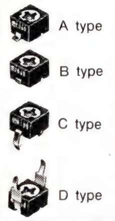

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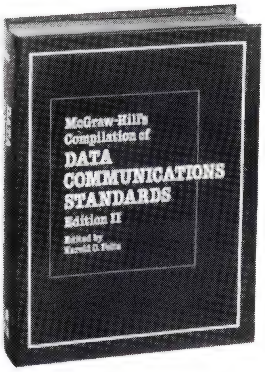
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HARRIS GOES AFTER DEC WITH A RISC ARCHITECTURE

Designed around Unix, the HCX-7 pumps out 7 mips with Schottky bit-slice logic

"We're set to put DEC out of business."

Rohit Kumbhani, marketing manager of CPUs and systems at Harris Corp., believes that his firm's enriched line of superminicomputers will be the key to capturing and dominating that marketplace—and take some of the boom out of Digital Equipment Corp.'s VAX thunder. The biggest selling point will be a reduced instruction set computer (RISC) architecture that will allow the new machine, built with Schottky bit-slice logic, to outperform the company's emitter-coupled-logic (ECL) computers. With the introduction today of two models—the HCX-7, the first in a new family of Unix-based 32-bit superminis, and the Model 1200, a real-time, ECL-based unit that extends the company's H-series on the high end—Kumbhani is confident that Harris can now accommodate the full superminicomputer user base.

The HCX family, he says, gives users a fast supermini for time-sharing environments that do not need the expensive real-time features offered by Harris's H-series, and also—unlike the company's work-station products—are capable of supporting a vast number of terminals. Designed to host Unix programs, the multiuser HCX-7 is Harris's way of "shooting for a greater share in the technical business market," says Kumbhani. He specifies education, research, general engineering, and some computer-aided design as target applications for the new model.

The star feature of the HCX family is its native AT&T Bell Laboratories Unix operating system. Rather than adapt Unix to an existing architecture, Harris designed the computer to run Unix. The idea is to "enable each product line to do what it does best," says Kumbhani, explaining that it is inefficient to try to shoehorn an operating system onto a computer that was not designed for it.

"You want to make the machine as simple as possible, to make it go as fast as possible," he says. That approach yielded a number of architectural features in the HCX-7 that permit the computer to achieve a speed of 7 million instructions per second. That speed varies between 4 and 10 mips, depending on the application program, Kumbhani points out. Although he acknowledges that mips is often said to stand for "Meaningless Information from Pandering Salesmen," he stresses that as one of the few benchmarks by which computers' performance can be compared, it does offer some valuable information. The HCX-7 processes instructions some 4 to 10 times faster than DEC's 1-mips VAX-11/780, he says, adding that it can also achieve as much as twice the speed of DEC's more recent 8600.

The fact that the HCX-7 uses Advanced Micro Devices Inc.'s Am2900 bit-slice chips rather than the faster ECL design used by its real-time cousins in the H-series is a tribute to a streamlined system in which 160 of the most common instructions—out of a normal set of 300 to 350—are implemented in system hardware. Harris screened out the more complex and redundant instructions to allow the RISC unit to perform Unix program commands at high speeds. Says Kumbhani: "If a machine is designed efficiently, it should not matter what application you are using, because any program will boil down to the same set of instructions. You can do everything possible within those instructions." RISC is winning adherents because of the speed gained by eliminating complex instructions that can be performed in other ways.

Because Harris is now pushing three distinct lines of superminicomputers, the natural question is, just how distinct are they? Will the Unix-based HCX-7 be able to communicate with H-series computers, which use Harris's proprietary VOS operating system? Not to worry, says Kumbhani. Harris has developed a modified operating system, VUE, that permits H-series computer users to work in both the VOS and Unix languages. The new operating system will run most Unix programs, Kumbhani says. In addition, Unix is already available on Harris's models 10 and 20 work stations. "Even though hardware may be different, there is a communality among the three computer lines," he says.

The HCX-7 uses a small CPU made up of five complex subsystems: an instruction processor, a control unit, an address generator, an address translator, and a data loop. Communicating with one another over a pair of 32-bit buses—one for memory and the other for I/O—the five boards rely on a three-stage pipeline capability that synchronizes CPU functions among the five so that three instructions can be processed concurrently. In effect, each board performs its individual function and then immediately off-loads the given instruction to the next component within the CPU.

For example, the instruction-processor board fetches and decodes an instruction and then instantly passes it along to the control unit and address regulator. While the next two boards calculate the address

and generate microcode words for the first instruction, the instruction processor is already decoding a second instruction.

HCX-7's independent cache memory layout has separate caches for instructions, data, and virtual memory. The instruction cache is 73 bits wide and stores 4,096 decoded instructions; the data cache can store 16-K bytes. Thanks to their isolated design, each can be accessed simultaneously, eliminating contention and again resulting in greater speed.

The system includes two cabinets, one housing the CPU, memory, systems interfaces, and a microprocessor dedicated to booting and debugging the system, and the other containing rack-mountable peripheral devices compatible with H-series systems. The basic HCX-7, which costs $225,000, consists of the CPU, 2 megabytes of memory, a console processor and terminal, an asynchronous controller, and a power supply. With another 2 megabytes of memory, a floating-point processor, and an I/O expansion cabinet, the price is $275,000. Up to 30 megabytes of additional memory can be added, as can two more peripheral cabinets, an I/O-controller expansion cabinet, and up to 25 additional I/O controllers. Fully expanded, the system supports 235 RS-232-C or RS-422 serial lines to terminals, printers, or other serial devices. *–Tobias Naegele*

Harris Corp., Computer Systems Division, 2101 W. Cypress Creek Rd., Ft. Lauderdale, Fla. 33309.
Phone (305) 974-1700 [Circle reader service number 338]

Spreadsheet program contains data base, produces graphics

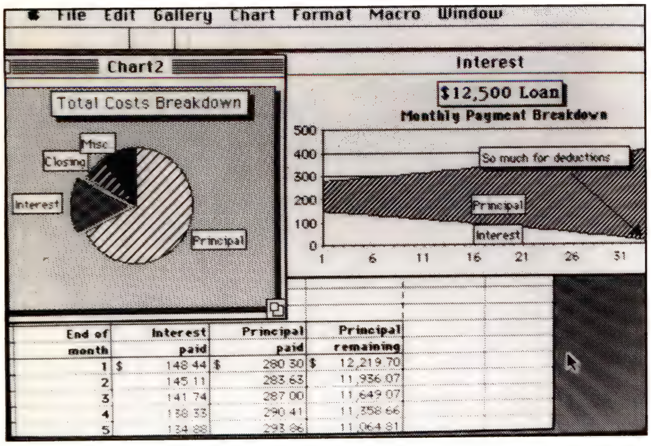
Business graphics and an on-sheet data base are combined in Excel, a spreadsheet that combines user-defined functions, array handling, and two-way file compatibility with the Lotus 1-2-3 program on the IBM Corp. Personal Computer, Multiplan and Chart on Macintosh, and Microsoft Sylk format (including Multiplan) on the IBM PC.

The worksheet is organized as 256 columns by 16,384 rows—over 4 million cells—and multiple worksheets can be interactively linked; variable fonts and font sizes present data within five border styles for individual cells or regions. When data are to be presented in a chart, the user can select from 42 built-in formats, adding legends and text at will. Multiple windows can also be opened.

Excel works with the Appletalk network; in an office that has IBM PCs and Macintoshes linked together, Excel can exchange files among compatible spreadsheets from either computer. It also supports Laserwriter, Imagewriter, and any connectable printer for text-only printing.

Excel will begin shipping in September. It runs on a 512-K Macintosh computer, and an external disk drive is recommended. The suggested retail price is $395, but owners of Multiplan can upgrade to Excel for $200, and owners of both Multiplan and Chart for the Macintosh can upgrade for $100. The Apple Switcher will be bundled with Excel.

Microsoft Corp., 10700 Northup Way, P.O. Box 97200, Bellevue, Wash. 98009. Phone (206) 828-7400 [Circle 344]



End of month	Interest paid	Principal paid	Principal remaining
1	$ 148.44	$ 280.30	$ 12,219.70
2	145.11	283.63	11,936.07
3	141.74	287.00	11,649.07
4	138.33	290.41	11,358.66
5	134.88	293.86	11,064.81

Circuit-design software uses spreadsheet tactics

Integrated engineering software for microwave-circuit design, Linecalc works like a spreadsheet to analyze physical parameters and display the corresponding electrical parameters. The program also synthesizes physical parameters after the design engineer specifies the desired electrical parameters. For coupled transmission lines, any two of four parameters—even-mode impedance, odd-mode impedance, characteristic impedance, and coupling—can be specified, and Linecalc automatically calculates the other two. Using the computer's function keys, the designer can enter new values or existing values can be incremented or decremented by 1% or 10%.

Linecalc uses the same transmission-line models as Touchstone, a computer-aided analysis and optimization program from the same company, and Linecalc's synthesis procedure also uses the same algorithms; results from Linecalc can thus be submitted to Touchstone.

As a stand-alone program included in the Touchstone package, Linecalc's price will be quoted by the manufacturer. Current owners of Touchstone receive Linecalc at no charge as an upgrade. The software runs on the IBM Corp. Personal Computer, PC/XT, PC AT, and compatibles, and will be available in the future for Hewlett-Packard Co.'s 200 series.

Eesof Inc., 31194 La Baya Dr., Suite 205, Westlake Village, Calif. 91362. Phone (818) 991-7530 [Circle 341]

Editing capabilities, new keys enhance terminal

Sixteen function keys upgrade the ADM 11plus video display terminal from its predecessor, the ADM 11. In addition, three editing keys and a break key can be programmed to supplement the basic 16. The ADM 11plus general-purpose terminal also has upgraded editing capabilities: character or line insert or delete, line erase, and page erase.

Also provided are four visual (nonembedded) attributes—reduced intensity, blink, blank, and reverse video—along with

a two-level English-language setup and a 25th (status) line. Options include international character sets, answer-back memory, and a 14-in. green or amber screen.

Available for shipment in June, the ADM 11plus is priced at $695 in single-unit quantities. It is compatible with several other terminals from the same manufacturer, the DEC VT52, Applied Digital Data Systems, and Hazeltine.

Lear Siegler Inc., 901 E. Ball Rd., Anaheim, Calif. 92805.
Phone (714) 778-3500 [Circle 348]

OCR scans documents, sends data to desktop computers

With a feature called Poorcopy, the Omni-Reader optical-character scanner package can handle even a photocopy of a photocopy, several copies removed from the original. The manufacturer has upgraded the scanner, which is already on the market, into a package containing an RS-232-C connector cable, the software to link it to IBM Corp. Personal Computers and compatibles or to the Apple Macintosh, and the Poorcopy feature.

At the rate of up to 180 words/min, Omni-Reader scans Courier 10, Courier 12, Letter Gothic, and Prestige Elite—all common typewriter fonts—while additional font selections for downloading to the unit will be released soon.

The Omni-Reader's overall dimensions (including tablet, short rule, and read head) are 4.8 in. by 10.7 in. by 16.0 in. It weighs 2.6 lb. Through the software interface, the Omni-Reader can transfer scanned data to word processing or other applications on most popular desktop computers. Machines without this interface can usually create an ASCII data file through common communications software.

The retail price of the bundled package is $799; an unbundled Omni-Reader, with Poorcopy and training certificate but without software and cable, is priced at $699. The scanners are available now.

Oberon USA Inc., MacArthur Plaza, Suite 630, LB48, 5525 MacArthur Blvd., Irving, Texas 75038. Phone (800) 262-3766 or (214) 257-0097 [Circle 349]

Controller chip works with any disk drive or system

Compatible with a wide range of standard disk-drive interfaces, the DP8466 Disk Data Controller is both drive- and system-independent. The device is programmable, so that it can control any number of drives and any mix of drive types. It can handle data-transmission rates up to 24 Mb/s and has programmable channel addressing for direct memory access.

Also included is a 32-byte first-in, first-out buffer, programmable error checking and correction, and disk-data and data-bus timing and control. Circuitry for serializing and deserializing data is also on-chip.

Compatible with any 8-, 16-, or 32-bit microprocessor, the DP8466 uses programmable polynomials of 32- and 48-bit length to perform internal error-checking and correction functions. It can make 8- or 16-bit data transfers.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, Calif. 95051. Phone (408) 721-5000 [Circle 368]

8-bit microcontroller supports data transfers of 500 kb/s

Built in Intel Corp.'s latest CMOS process, CHMOS III, the 80C51BH-1 8-bit microcontroller can operate at frequencies of up to 16 MHz, making it a potentially powerful tool in storage drives and modems.

Features include a Boolean processor for bit-level data manipulation, 32 programmable I/O ports, programmable power modes, and a universal asynchronous receiver/transmitter port. Also included on-chip are 4-K bytes of ROM and 128 bytes of RAM. Intel claims these features combine with the 80C51BH-1's speed to give the part the highest all-around performance of any 8-bit microcontroller available.

A 4- to 6-V power source can run the device, which needs an operating current of 20.5 mA—less than 50 μA on standby. At full speed, the microcontroller can support data-transfer rates of up to 500 kb/s. In orders exceeding 5,000 units, the microcontroller is priced at $11.55.

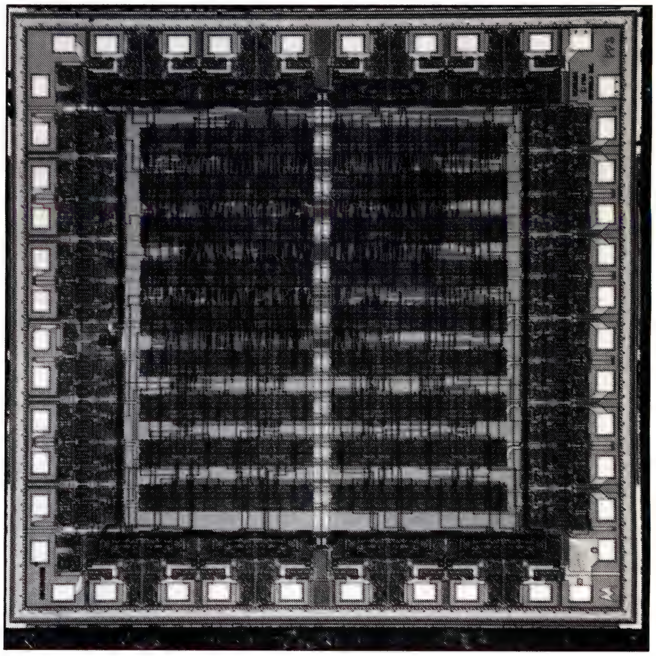
Intel Corp., 5000 W. Williams Field Rd., Chandler, Ariz. 85224.
Phone (602) 961-2756 [Circle 379]

Chip replaces ports lost by microcomputer's special modes

Implemented by means of a 600-gate semicustom logic array, Motorola Inc. has quickly completed design of a new processing peripheral circuit that replaces or expands I/O ports of 8-bit microcomputer chips. The peripheral is aimed at integrating the functions needed to replace two 8-bit parallel I/O ports whenever microcomputers—especially the Motorola MC68HC11—are used in an expanded off-chip memory mode or special test modes.

Fabricated in Motorola's own high-performance n-MOS silicon-gate logic arrays, the MC68HC24 supports all the handshake signals and I/O modes of the 68HC11. It is also being marketed as a low-cost circuit for I/O expansion, parallel-printer interface, and interprocessor communications for a wide range of CMOS microcomputers.

The Microcomputer Operation of Motorola's Microprocessor Products Group created the new 8-bit peripheral, routing all the gates on the 600-gate array. The result is a 40-pin port-replacement unit, which in a plastic DIP costs $16 each for



quantities of 1,000. The 68HC24 port replacement will also be available in a ceramic DIP costing $20.50 each, and a surface-mountable 44-pin plastic-leaded chip carrier, selling for $16 each. Samples units are now available, with production quantities slated to begin in the third quarter.

The 68HC24, which supports 0-to-2.1-MHz operation and runs on a 3.0- to 5.5-V power supply, has a multiplexed address/data bus. It has been tailored to conform automatically to the variable memory map of the 8-bit 68HC11. Port B on the 68HC24 is a general-purpose output channel, with fixed data direction, which emulates the port B on the 68HC11. Port C is a general-purpose I/O port. The maximum power dissipation of the port-replacement unit is 25 mW.

Motorola Microcomputer Operation, William Cannon at U.S. Rte. 290 W., P.O. Box 6000, Austin, Texas 78762.
Phone (512) 440-2035 [Circle 381]

Computer family adapts to user's storage needs

Three entry-level computers, available in three configurations, have been added to the MC-186 line of multiuser systems. All MC-186 systems support the MC-Net network option so that the MC-186 can be connected with up to 255 multiuser systems, the IBM Corp. Personal Computer and compatibles, or the ACT Computers Inc. Apricot.

The system 62/A, with one 5¼-in.-floppy-disk drive, 62 megabytes of hard-disk storage, and 1 megabyte of RAM, contains 10 RS-232-C serial ports and is priced at $14,995. System 62/C has one 5¼-in.-floppy-disk drive, one 5-megabyte removable hard-disk drive, 62 megabytes of hard-disk storage, 1 megabyte of RAM, and 10 RS-232-C serial ports. Its price is $16,695. Other configurations are priced from $8,995.

The machines' operating system is MC-DOS, the manufacturer's enhanced implementation of Concurrent DOS. MC-DOS is a multiuser, multitasking, networking, real-time operating system that can run both 8- and 16-bit single- and multiuser CP/M applications.

Gifford Computer Systems, 2446 Verna Ct., San Leandro, Calif. 94577. Phone (415) 895-0798 [Circle 340]

Memory subsystem combines storage and backup devices

For $2,995, owners of IBM Corp. Personal Computer ATs, PC/XTs, and compatibles can expand their systems with a compact external memory system called Microstor.

Measuring 16 by 8 by 5 in., the memory enhancement unit combines a 5¼-in. 20-megabyte (formatted) Winchester disk drive and a 23-megabyte streaming-tape backup unit to improve memory capacity, while requiring just a single controller card to run effectively, the company says.

Microtip, a software program for complete file-oriented back-up and restoration of data, is included with the unit.

Alloy Computer Products Inc., 100 Pennsylvania Ave., Framingham, Mass. 01701. Phone (617) 875-6100 [Circle 356]

8-in. hard-disk drive boasts 337-megabyte capacity

Manufacturers seeking high-performance disk drives for multiuser and multitasking systems can use the D2268 8-in. Winchester disk drive. Providing up to 337 megabytes of storage, the unit performs data transfers at 1.86 megabytes/s and typically accesses data in 20 ms.

The D2268 puts out detailed error reports and features address-mark detection and an automatic head-carriage lock to protect data during handling and shipment. The drive has an extended-storage-module-device (ESMD) interface to ease integration with readily available controllers and can be purchased with an optional dual port.

Complete with a mounting frame bracket, the D2268 is priced at less than $4,000 in original-equipment-manufacturer quantities. Evaluation samples can be delivered 30 to 60 days from receipt of order.

NEC Information Systems Inc., 1414 Massachusetts Ave., Boxborough, Mass. 01719. Phone (617) 264-8000 [Circle 354]

20-megabyte Winchester drives come in three configurations

Designed for use with the IBM Corp. Personal Computer AT, the MI25 trio of 5¼-in. Winchester disk drives and the MT23 tape drive offer several choices to expand memory capacity.

The 20-megabyte MI25 hard disk drive comes in three configurations: an initial drive and mounting bracket that fits into the PC AT, a 40-megabyte dual drive, and an add-on drive that mounts on the initial Winchester to double capacity.

The 23-megabyte MT23 half-height cartridge tape drive is a file-oriented backup for PC ATs with hard disk drives and fits where a second hard disk or a floppy-disk drive would otherwise be mounted. The unit allows individual file backup and restoration, the company says.

Including cables, mounting, and the necessary tools for installation, the price of the MI25 is $1,095 for the initial 20-megabyte configuration, $995 for the add-on drive, and $2,090 for the 40-megabyte dual unit. The MT23 costs $795. The memory units are available now.

Microsystems International Corp., 100 Pennsylvania Ave., Framingham, Mass. 01701. Phone (617) 875-9700. [Circle 355]

Portable digital multimeter gives true RMS measurements

Compact and versatile, the model 4740 digital multimeter performs a variety of tests: ac/dc voltage and current, resistance, frequency, dBm, diode and continuity check, and temperature. The portable unit features data hold, peak hold, a relative display, and autoranging.

The 4½-digit meter offers a 3½-digit display mode; a custom large-scale integrated circuit is used to provide a 25,000-count resolution. True root-mean-square measurement capability suits the 4740 for either field or laboratory testing of a range of commercial and industrial equipment.

Users can select either autorange or manual range: in manual range, a relative-measurement mode is available in all voltage, current, and resistance ranges that stores the applied input as a zero reference point. Subsequent measurements are then displayed as deviations from the stored value.

Ranges included are dc voltage from 0 to 1,000 V in five ranges; ac voltage from 0 to 750 V in five ranges; current from 0 to 10 A in two ranges; resistance from 0 Ω to 25 MΩ in six ranges; continuity check at 250 Ω; frequency from 10 Hz to 100 kHz in four ranges; forward-voltage diode test from

0 to 2.5 V; power level from –50 dBm to 60 dBm in four ranges; and temperature from –50°C to 1,200°C.

Multiple-fuse overload protection is provided, as is an internal 9-V dc battery, safety test leads, spare fuses, a bench stand, and a comprehensive instruction manual. Optional accessories, including an ac adapter, are also available. The unit is priced at $340 and will be available in July from stock.

Triplett Corp., 1 Triplett Dr., Bluffton, Ohio, 45817.
Phone (419) 358-5015 [Circle 360]

Generator puts out video signals at 200 million pixels/s

Because the Opix Imager, a video signal generator, stores images as individual pixels rather than as characters, it can display anything that can be drawn with paper, pencil, and template directly on a CRT.

The signal generator, moreover, treats text as graphics, permitting text and full-color graphics to coexist within an image and allowing unconstrained use of differing fonts and type sizes. The generator, which is useful in evaluating high-resolution raster-scanned products and signal formats, allows users to enter the physical size of an image as well as the amount of horizontal and vertical resolution desired, and then automatically scales the image.

Digital video signals are ouput at 200 million pixels/s and digital data flows at 1.6 Gb/s. Analog video output is rated at up to 125 million pixels/s. Of the 18 output ports, 15 are digital and 3 are analog. Every output is brought out differentially, and each digital signal is output as both TTL and ECL-compatible pairs.

The Opix Imager, housed in a 5¼-by-17-by-16¾-in. package that includes an 80-character LCD display, has two RS-232-C serial ports—one for connection to a terminal, and one for a printer or plotting device. Also included are 1.5 Mb of memory and four synchronous channels. Pricing for the Opix Imager is set at $12,500, and it is available now.

Quantum Data Inc., 455 E. Kehoe, Carol Stream, Ill. 60188.
Phone (312) 668-3301 [Circle 362]

64-channel logic analyzer does both timing and state analysis

Timing and state analysis of very high-speed ICs, fast-state machines, and supercomputers are performed on the 64-channel model 2230 logic analyzer. Each channel features 125-MHz synchronous clocking, and each can be used interchangeably for either timing or state tests to capture glitches as narrow as 3 ns.

Using an external asynchronous clock, timing analysis can be performed on any channel at up to 125 MHz; the internal clock permits analysis at up to 100 MHz. Eight channels are also sampled at 400 MHz to provide 2.5-ns resolution.

Bugs can be isolated in either complex multiple-path programs or logic by up to 64 linkable conditional branch triggering instructions. Pricing is from $11,970 to $18,975. Delivery takes two weeks.

Intech Inc., 282 Brokaw Rd., P.O. Box 58064, Santa Clara, Calif. 95052. Phone (408) 727-0500 [Circle 361]

Dot-matrix printer pumps out 400 characters/s

Speed is the key to the Model 3410 serial dot-matrix printer, which not only boasts a 400 characters/s data-processing print speed, but can also print letter-quality text and high-resolution graphics.

The printer's 18-wire printhead offers resolution of 72 or 144 dots/in., and spits out pica-sized letter-quality text at 100 characters/s. The user can choose expanded, emphasized, double-strike, or oversize characters. Courier is the standard typeface, but a variety of fonts are available as an option. Graphics are printed at a 15-in./s slew rate.

Both serial and parallel interfaces are included, and the unit supports IBM Corp. Personal Computer graphics and ANSI X3.64 protocols. Users thus have complete control of the printer from their computer keyboards. Available now, the 3410 dot-matrix printer costs $2,450.

Genicom Corp., 1 General Electric Dr., Waynesboro, Va. 22980.
Phone (703) 949-1000 [Circle 363]

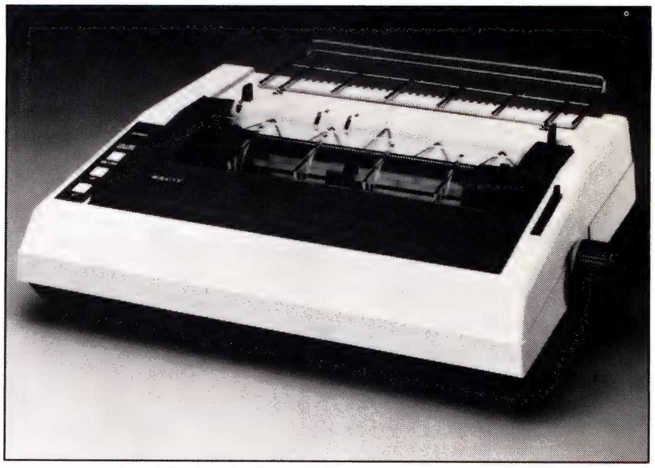
Dot-matrix printer for IBM PC prints text at 120 characters/s

Claiming all the features of the standard IBM Corp. Personal Computer printer, the 4509 dot-matrix printer is compatible with all standard software packages in its IBM/Epson mode. It may also be used with other computers when set in its RX-80 mode.

The 80-column unit prints 120 characters/s at 57 dB, and when set for the double-pass mode, it can achieve high resolution, the company says. Users can choose pitches of 10, 12, or 17 characters/in., as well as standard, boldface, italicized, elongated, and underlined type styles. Graphics reproduction has three resolution settings: 60, 120, and 240 dots/in.

The $495 printer's printheads, which are easily changed, will last for more than 100 million characters or several years of normal use, the manufacturer says. The 4509 is available immediately from stock.

Facit Inc., 9 Executive Dr., Merrimack, N.H. 03054 [Circle 365]



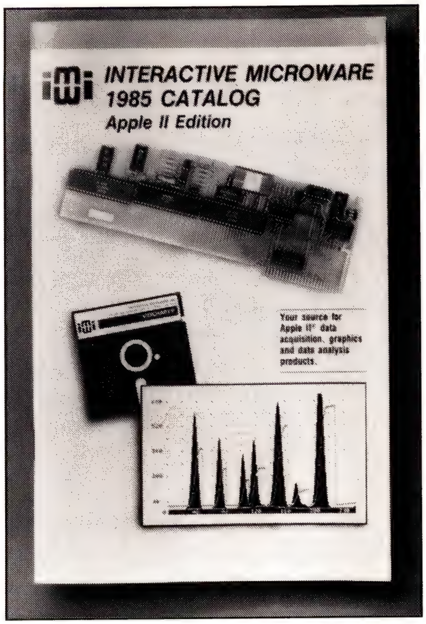
Countdown. Counters, sensors, hour-meters, and controls are the offerings in the 12-page catalog from Redington Counters Inc. Products featured include the 7600 series of miniature LCD-type panel-mount totalizers, tachometers, and hour-meters, the 9600 series of ac and dc proximity sensors, and the 9500 series of electronic predetermining counters. For a free copy, call (203) 688-6205 or write to the company at 130 Addison Rd., P.O. Box 608, Windsor, Conn. 06095. [Circle reader service number 422]

Sweet talk. Voice and data wiring systems for one or several buildings in a campus-type setting are described in this free brochure, entitled "Private Network Products." The brochure describes the components of such a system, including distribution terminal, riser cable products, underground splices or closures, and cabinets. Request it from TelComm Products Division/3M, Dept. TL85-19, P.O. Box 33600, St. Paul, Minn. 55133. [Circle 423]

Show and tell. Long-life LCD displays for outdoor use and in extremely high- or low-temperature environments are covered by a free data sheet from LXD Inc. According to the company, sample units were still running after 2,000 h exposure to dry heat at 90°C. The data sheet also details custom design and prototype services for designers of LCD displays. Interested parties should ask for Product Data Sheet 101, "Long Life Liquid Crystal Displays." The address is 24500 Highpoint Rd., Beachwood, Ohio 44122—or call (216) 292-3300. [Circle 424]

Read all about it! Sample copies of "The Programmer," which is called the programmable controller newsletter for the small-system designer, are free on request. A sequencing program adapted from a drum counter and descriptions of on-delay and off-delay timers are examples of information featured; and each issue contains ladder-logic programs with step-by-step explanations, and hints for program documentation and debugging. "The Programmer" is published by Automated Control Systems, P.O. Box 23021, Richfield, Minn. 55423. Phone (612) 869-0072. [Circle 425]

Apple II analysis. Data-acquisition hardware and analysis software for Apple II personal computers are described in this 64-page catalog, which is aimed at science, engineering, and business professionals. The complete line includes the general-purpose Adalab data-acquisition interface card and hardware accessories; software for graphics plotting, drafting, and design; software for multichannel, multipurpose data logging and process control; and many other supplies and accessories for the Apple II. To receive a free copy, call Interactive Microware Inc. at (814) 238-8294, or write to P.O. Box 139, State College, Pa. 16804. [Circle 421]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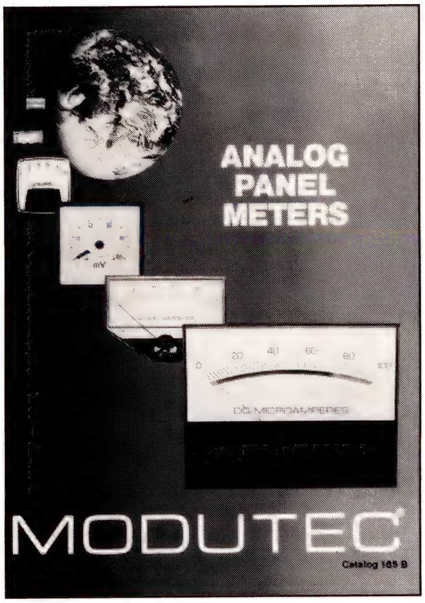
Cramped quarters. A space-saver line of analog panel meters is featured in this 64-page catalog, issued by Modutec Inc., with photographs on a scale of 1:1 and dimensional drawings to aid designers in specifying units. The space savers feature an insulated barrel and a choice of several European and U.S. mounting-stud configurations; diffused backlighting is optional. Request catalog 185B when calling (800) 638-3771, or write to 18 Marshall St., P.O. Box 778, Norwalk, Conn. 06856. [Circle 426]



High jump. Jump Jax are miniature jumper and shorting jacks, with a ring contact—beryllium copper-plated—that deforms into an ellipse on insertion for maximum force on the pins. Jump Jax are rated for up to 500 insertions and withdrawals with no electrical degradation, the manufacturer says. Four styles are available, and they are fully specified in a catalog that is free for the asking from Sealectro Corp., 40 Lindeman Dr., Trumbull, Conn. 06611. Phone (203) 372-4118. [Circle 427]

Turn up the heat. A hand-held intelligent infrared thermometer, the Raynger II calculates an on-line average with an accuracy of 0.1°F or °C for temperatures below 1,000°F or 500°C. A brochure from the manufacturer, Raytek Inc., describes the instrument's microprocessor technology and applications, such as process monitoring and maintenance diagnostics. Data is held in memory when the logic switches to standby mode, and an optional scope permits sighting on targets as small as 0.2 in. from a distance of 12 in., the literature says. The Raynger II connects to data-acquisition systems and chart recorders. The brochure is sent free on request from 1201 Shaffer Rd., Santa Cruz, Calif. 95060. Phone (800) 227-8074 or (408) 458-1110. [Circle 430]

Chip shot. A chip carrier formulated in custom polyimide multilayer structures, for use with high-speed GaAs ECL or CMOS parts, is described in Bulletin 103 from Augat Microtec. Titled "Leaded Polyimide Chip Carriers," the bulletin specifies the manufacturer's high-performance type (PHIP) and high I/O count type (PHIL). The PHIP model features controlled impedance lines, low capacitance, and low inductance. The free literature is available by calling 498-9643 or writing to the Marketing Dept. at 2520 Turquoise Circle, Newbury Park, Calif. 91320. [Circle 428]

Well developed. What is a good development system? This brochure from Computer Dynamics answers in terms of the manufacturer's microfloppy-disk development systems for the STD bus. The standard system offered is based on the Z80 CPU running at 4 MHz (6 MHz is optional), fits on a desk top, incorporates the drives and power supply into the card cage, and delivers 760-K bytes of storage on a 3½-in. microfloppy disk encased in hard plastic—recommended for industrial systems. For the balance of what's offered in this package, ask for the brochure at (803) 877-7471. The mailing address is 105 S. Main St., Greer, S.C. 29651. [Circle 429]

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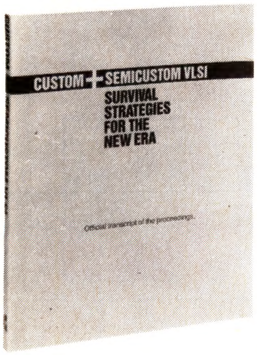
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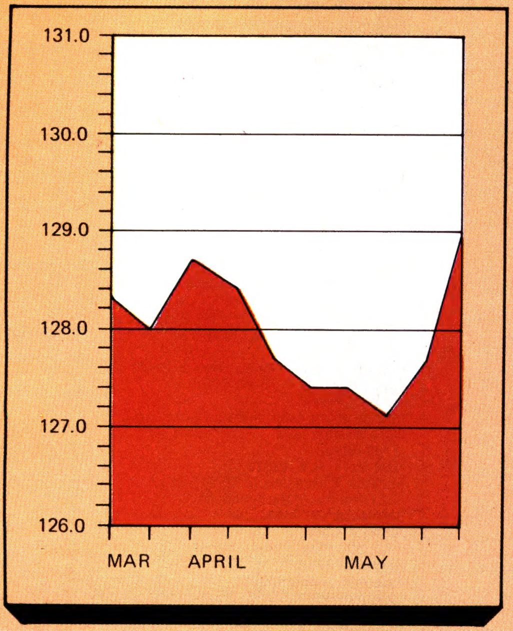
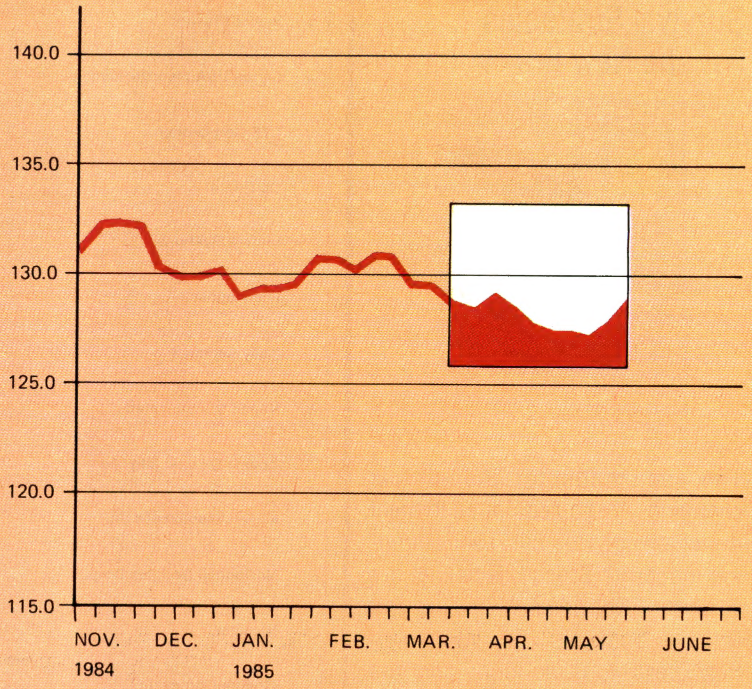
ELECTRONICS WEEK INDEX





THIS WEEK = 129.0
LAST WEEK = 127.7
YEAR AGO = 124.5
1982 = 100.0

The *ElectronicsWeek* Index, a seasonally adjusted measure of the U.S. electronics industry's health, is a weighted average of various indicators. Different indicators will appear from week to week.

U.S. ELECTRONICS IMPORTS AND EXPORTS ($ MILLIONS)

	IMPORTS			EXPORTS		
	March 1985	**February 1985**	**March 1984**	**March 1985**	**February 1985**	**March 1984**
Accounting, computing, and data-processing machines	342.244	315.364	281.551	783.125	554.215	596.159
Calculators	56.763	44.680	50.282	9.460	6.456	7.305
Parts for data-processing machines and office calculators	369.056	334.806	371.769	696.167	525.948	535.475
Telecommunications, sound-recording, and sound-reproducing equipment	1,661.969	1,280.576	1,226.448	467.097	313.910	362.427
Electronic or electric instruments	154.784	116.282	128.756	694.551	499.021	573.726
Printed-circuit boards	24.637	26.409	16.523	29.525	24.354	22.615
Integrated circuits, diodes and other semiconductors, tubes, piezoelectric crystals, parts	653.302	555.513	816.056	522.980	374.245	502.367
Fixed and variable resistors	24.628	22.567	25.739	15.253	11.761	15.804

Exports rebounded vigorously, driving the *ElectronicsWeek* Index to its highest level in two months. The 39.3% surge boosted the index 1.3 points, despite a 21.9% increase in electronics imports. What's more, the export explosion cut the domestic industry's trade deficit to $69 million in March from $386 million the previous month.

Electronics manufacturers virtually across the board made healthy inroads in overseas markets in March; every product group boosted exports at least 20%. Printed-circuit boards, the industry segment with the smallest increase, saw exports increase 21.1% in March. The largest gain was in the telecommunications industry, in which exports climbed nearly 50%.

The largest increase in imports came from foreign instruments manufacturers who upped shipments into the U.S. by 33%. Less substantial though significant inroads came from foreign telecommunications and semiconductor manufacturers with gains of 30% and 18%, respectively.

With the recent decline in the prime interest rate to 10%, industry leaders hope the U.S. exchange rate will drop enough to give a trade surplus back to the domestic electronics industry.

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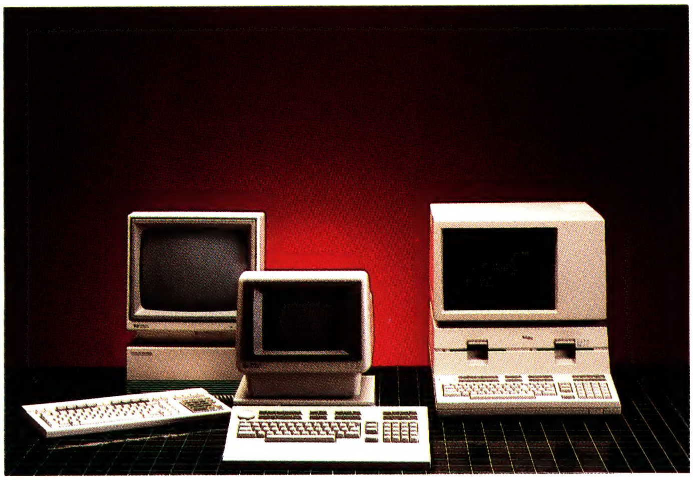

Pictured: Hewlett-Packard 200 Series Computers

- All BASIC 3.0 statements and extensions are supported.
- Typical integer performance is improved by a factor of 10 – 30. Real performance by a factor of 6 – 10.
- Compiled programs interface directly with Infotek math cards.
- Flexible directives permit program optimization.
- Compiled code provides user program security.

BASIC 3.0 INTEGER PERFORMANCE SPECIFICATION

STATEMENT	INTERPRETED BASIC	COMPILED BASIC	PERFORMANCE RATIO
FOR...NEXT	67	10	6.7
REPEAT...UNTIL	282	4	70.5
WHILE...END WHILE	479	6	79.8
IF...THEN	289	5	57.8
SELECT...CASE	1056	14	75.4
A = B	130	3	43.3
A = B + C	198	6	33.0
A = B − C	198	6	33.0
A = B * C	203	11	18.5
A = B DIV C	216	25	8.6
A = NOT B	213	6	35.5
A = B AND C	301	8	37.6
A = B OR C	307	8	38.4
A = B EXOR C	309	10	30.9
A = Array(B)	253	11	23.0
A = Array(B,C)	325	24	13.5
A = ABS(B)	163	6	27.2
A = SGN(B)	222	8	27.8
A = BINCMP(B)	255	5	51.0
A = BINAND(B,C)	300	6	50.0
A = BINIOR(B,C)	300	6	50.0
A = BINEOR(B,C)	300	6	50.0
A = ROTATE(B,C)	303	10	30.3
A = SHIFT(B,C)	306	10	30.6
A = BIT(B,C)	305	10	30.5

Performance numbers are in microseconds and represent typical execution times for Interpreted and Compiled BASIC

BASIC 3.0 REAL PERFORMANCE SPECIFICATION

STATEMENT	INTERPRETED BASIC	COMPILED BASIC	PERFORMANCE RATIO
FOR...NEXT	183	47	3.9
REPEAT...UNTIL	343	10	34.3
WHILE...END WHILE	540	12	45.0
IF...THEN	307	23	13.3
SELECT...CASE	1216	36	33.8
A = B	134	9	14.9
A = B + C	289	40	7.2
A = B − C	306	41	7.5
A = B * C	451	42	10.7
A = B / C	583	47	12.4
A = NOT B	207	30	6.9
A = B AND C	237	33	7.2
A = B OR C	270	35	7.7
A = B EXOR C	258	37	7.0
A = Array(B)	256	18	14.2
A = Array(B,C)	327	31	10.5
A = ABS(B)	174	12	14.5
A = SGN(B)	241	35	6.9
A = SQR(B)	2051	217	9.5
A = SIN(B)	4327	475	9.1
A = COS(B)	4626	533	8.7
A = TAN(B)	4406	480	9.2
A = ASN(B)	5514	593	9.3
A = ACS(B)	5509	596	9.2
A = ATN(B)	4550	496	9.2
A = EXP(B)	3744	455	8.2
A = LOG(B)	4044	469	8.6
A = LGT(B)	4309	496	8.7
A = B^C	6967	960	7.3

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Pictured: BC 203 BASIC Language Compiler software with FP 210 Floating Point Coprocessor

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